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Atomic Layer Deposited Beryllium Oxide as a Gate Dielectric or Interfacial Layer for Si and III-V MOS Devices

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Atomic Layer Deposited Beryllium Oxide as a Gate Dielectric or Interfacial Layer for Si and III-V MOS Devices

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Dedication

To my Lord for his greatness and dedicated guide to my belief toward true and perfect knowledge

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Atomic Layer Deposited Beryllium Oxide as a Gate Dielectric or Interfacial Layer for Si and III-V MOS Devices

Jung Hwan Yum, Ph.D.
The University of Texas at Austin, 2012

Supervisor: Sanjay K. Banerjee

The continuous improvement in the semiconductor industry has been successfully achieved by the reducing dimensions of CMOS (complementary metal oxide semiconductor) technology. For the last four decades, the scaling down of physical thickness of SiO_2 gate dielectrics has improved the speed of output drive current by shrinking of transistor area in front-end-process of integrated circuits. A higher number of transistors on chip resulting in faster speed and lower cost can be allowable by the scaling down and these fruitful achievements have been mainly made by the thinning thickness of one key component - Gate Dielectric - at Si based MOSFET (metal-oxide-semiconductor field effect transistor) devices. So far, SiO_2 (silicon dioxide) gate dielectric having the excellent material and electrical properties such as good interface (i.e., $D_{it} \sim 2\text{x}10^{10}$ $eV^{-1}cm^{-2}$), low gate leakage current, higher dielectric breakdown immunity (≥10MV/cm) and excellent thermal stability at typical Si processing temperature has been popularly used as the leading gate oxide material.

The next generation Si based MOSFETs will require more aggressive gate oxide scaling to meet the required specifications. Since high-k dielectrics provide the same capacitance with a thicker film, the leakage current reduction, therefore, less the standby power consumption is one of the huge advantages. Also, it is easier to fabricate during

the process because the control of film thickness is still not in the critical range compared to the same leakage current characteristic of SiO_2 film. HfO_2 based gate dielectric is considered as the most promising candidate among materials being studied since it shows good characteristics with conventional Si technology and good device performance has been reported. However, it has still many problems like insufficient thermals stability on silicon such as low crystallization temperature, low k interfacial regrowth, charge trapping and so on. The integration of hafnium based high-k dielectric into CMOS technology is also limited by major issues such as degraded channel mobility and charge trapping. One approach to overcome these obstacles is using alternative substrate materials such as SiGe, GaAs, InGaAs, and InP to improve channel mobility.

High electron mobility in the III-V materials has attracted significant attention for a possible application as a channel material in metal/oxide/semiconductor (MOS) transistors. One of the main challenges is that III-V MOSFETs generally lack thermodynamically stable insulators of high electrical quality, which would passivate the interface states at the dielectric/substrate interface and unpin the Fermi level. To address this issue, various dielectric, such as Si/SiO_2, Ge, SiGe, SiN and Al_2O_3, were considered as an interface passivation layer (IPL). Atomic Layer Deposited (ALD) Al_2O_3 has demonstrated superior IPL characteristics compared to the other candidates due to its high dielectric constant and interface quality. However, defect density in Al_2O_3 is still too high even as several cleaning methods such as NH_4OH, $(NH_4)_2S$ and F treatment have been developed, which limits the performance of III-V MOSFETs.

In the first part of this study, theoretical approaches to understand the motivation and requirements as an high-k gate dielectric or interfacial layer, and properties of ALD beryllium oxide (BeO) for Si and III-V MOS devices have been investigated. The second part of this study focuses on the precursor synthesis and fundamental material characterization of ALD BeO thin film using physical, optical and electrical analysis. Film properties such as self-cleaning reaction and oxygen diffusion barrier will be presented. At the third part, depletion mode transistor and self-aligned MOSFETs using ALD BeO on Si and InP high mobility substrates have been investigated. And as for the final part of this study, the density functional theory of $Be(CH_3)_2$ precursor, electromagnetics, and thermodynamics were investigated to understand the reaction mechanism and self-cleaning reaction, and to evaluate the gate dielectrics such as Al_2O_3, BeO, SiO_2, and HfO_2.

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CHAPTER 1: Introduction

1.1 High-k Gate Dielectrics in Compound Semiconductor FETs for Scaling and Performance

The continuous improvement in the semiconductor industry for the last 40 year has been achieved by reducing dimensions of complementary metal-oxide-semiconductor (CMOS) technology. For the last four decades, scaling down of physical thickness of SiO_2 gate dielectric has improved the speed and output drive current by shrinking of transistor area in integrated circuits. A higher number of transistors on chip, resulting in faster speed and lower cost is allowed by scaling down and these fruitful achievements have been made in part by the thinning the gate dielectric in Si based metal-oxide-semiconductor field effect transistors (MOSFET). Till recently, silicon dioxide (SiO_2) gate dielectric having the excellent material and electrical properties such as good interface (i.e., $D_{it} \sim 2x10^{10}$ $eV^{-1}cm^{-2}$), low gate leakage current, high dielectric breakdown field (≥10MV/cm) and excellent thermal stability at typical Si processing temperature has been used as the leading gate oxide material.

Current and next generation Si-based MOSFETs require more aggressive gate oxide scaling to meet the specifications. Since high-k dielectrics provide the same capacitance with a thicker film, the leakage current reduction, therefore, less standby power consumption is one of the advantages. Also, it is easier to fabricate during the process because the control of film thickness is still not in the critical range compared to SiO_2 film with the same leakage current characteristics. HfO_2 based gate dielectric is considered as the most promising candidate among materials being studied since it shows good characteristics with conventional Si technology and good device performance has been reported [1, 2]. However, it has still many problems like insufficient thermal stability on silicon such as low crystallization temperature, low-k interfacial layer regrowth, charge trapping and so on. The integration of hafnium-based high-k dielectric in CMOS technology is also limited by major issues such as degraded channel mobility and charge trapping. One approach to overcome these obstacles is using alternative substrate materials such as SiGe, GaAs, InGaAs, and InP to improve channel mobility.

High electron mobility in the III-V materials has attracted significant attention for a possible application as a channel material in metal/oxide/semiconductor (MOS) transistors. One of the main challenges is that the III-V MOSFETs generally lack thermodynamically stable insulators of high electrical quality, which would passivate the interface states at the dielectric/substrate interface and unpin the Fermi level. To address this issue, various dielectric, such as Si/SiO_2[3,4], Ge[5], SiGe, SiN and Al_2O_3[6], were considered as an interface passivation layer (IPL). Atomic Layer Deposited (ALD) Al_2O_3 has demonstrated superior IPL characteristics compared to other candidates due to its high dielectric constant and interface quality. Fig 1 shows the schematic MOS structures for device performance comparison without/with IPL. ALD Al_2O_3 improves the interface quality between high-k and channel layers. However, defect density in Al_2O_3 is still too high even as several cleaning methods such as NH_4OH, $(NH_4)_2S$ and F treatment have been developed [7], which limits performance of III-V MOSFETs.

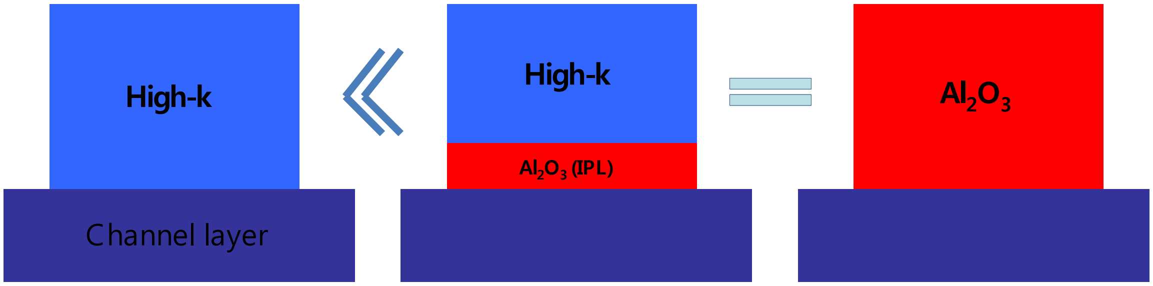


Fig 1. Schematic MOS structures for device performance comparison without/with IPL.

1.2 Requirements for IPL on Si and III-V MOS Devices

Based on prior studies, an ideal IPL is expected to satisfy several requirements. 1. *High thermal stability*: determined by the materials' Gibb's free energy [8] (See Table I). 2. *Large energy band gap*: Higher band gap dielectrics generally show better interface quality. 3. *Efficient diffusion barrier*: to prevent the gate dielectric contamination by the III-V channel materials. During thermal treatment, atoms such as In, Ga or As may diffuse into the dielectric and degrade the interface quality. A diffusion barrier has to have a sufficiently small dimension of the interstitial sites of the dielectric structure compared to the effective radii of In, Ga or As ions. 4. *Self-cleaning effect*: It depends on the chemical structure of the dielectric precursor. For example, the Al_2O_3 precursor, $Al(CH_3)_3$, absorbs oxygen from the native oxides such as Ga-O, As-O and In-O[8] due to high reactivity of the methyl ligand, CH_3, which shows better self-cleaning effect than Ethyl, C_2H_5. Self-cleaning effect depends on the chemical composition of precursor. 5. *Low density of structural defects at the interface*: This may also include oxygen vacancies and its associated stacking faults. Structural defect is due to the size difference between anion and cation. Metal cation and oxygen anion should be similar in size and, covalent bonding is preferable due to high bond strength. For examples, Hf atom is larger than oxygen atom in HfO_2, so oxygen is easily interstitial and it makes an oxygen vacancy and stacking fault. 6. *Low phonon scattering*: Scattering by the optical phonons and remote phonons may contribute to mobility degradation. BeO is characterized by relatively low phonon frequency with its high bond strength and band-gap which make hard to excite. 7. *No "d" orbitals*: Dielectrics with atoms which have d orbital usually have high DOS, which may lower band offset at the interface [10] and generate the multiple phase of oxidation states such as HfO_2 and Hf_2O_3 [11]. Hf_2O_3 is the theoretical source of oxygen vacancy in HfO_2.

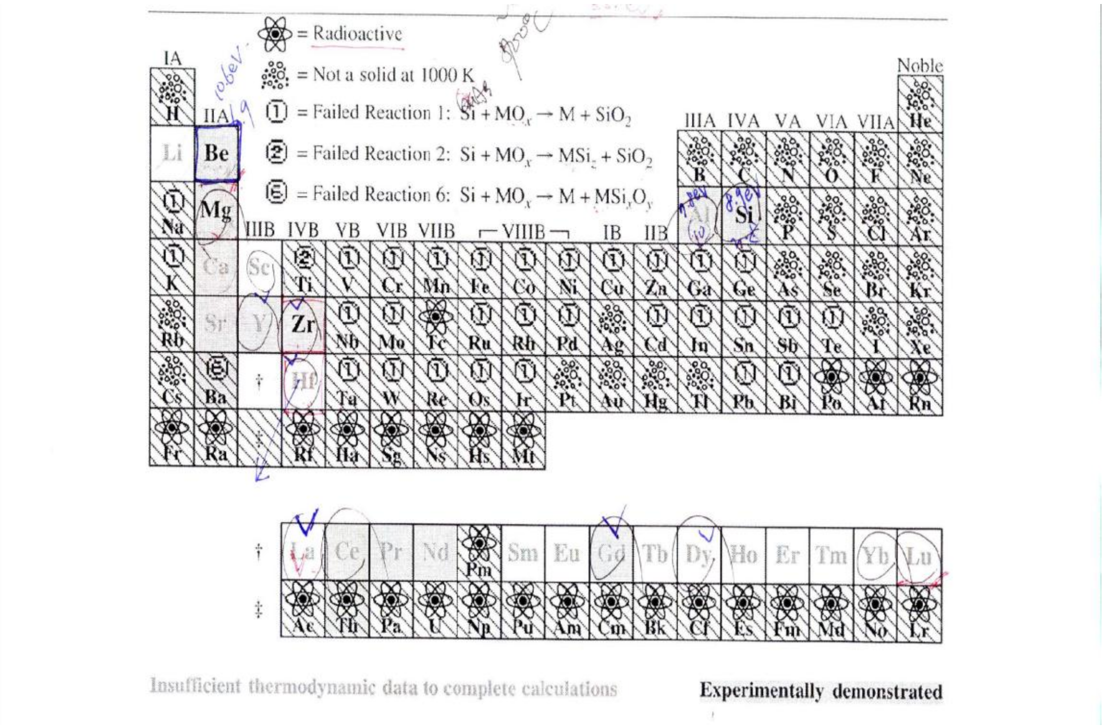


Table I. Binary oxides that were deemed unacceptable for integration with silicon at a growth temperature of approximately 1000 K [8].

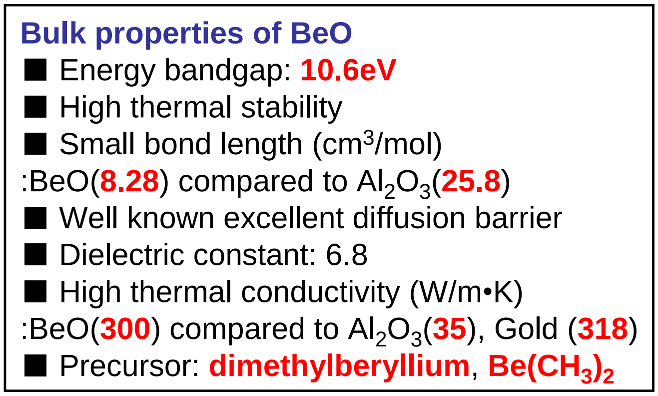
1.3 Introduction of Gate Dielectric Beryllium Oxide

On the basis of above requirements, beryllium oxide (BeO) was selected as a potential IPL for the III-V MOS devices. BeO has excellent thermal stability in contact with both Si and III-V substrates, in agreement with the value of its Gibbs free energy [8]. The energy band-gap of bulk BeO is 10.6eV [12], which is among the largest and its dielectric constant is around 6.8 [13], which is very close to that of ALD Al_2O_3 (about 7.1). Beryllium (Be atomic number: 4) does not have filled p orbitals, resulting in its small atomic radius. Beryllium oxide is well known to act as a strong diffusion barrier due to its very small Be-O length and dense structure with small interstitial spaces as well as a strong covalent bonding due to a similar electronegativity of Be and O. BeO causes low remote phonon scattering in the channel due to its compared to other dielectrics. The low phonon frequency also leads to high thermal conductivity in BeO compared to other dielectrics. The thermal conductivity of BeO at room temperature is 300 $W \cdot m^{-1}K^{-1}$ (while for alumina, it is 35 $W \cdot m^{-1}K^{-1}$), which can lead to efficient heat dissipation near the MOSFET drain edge.

1.4 Importance of Be and BeO and their Bulk Properties

Beryllium is an effective p-type dopant in III-V compound semiconductors. It is widely used in materials such as GaAs, AlGaAs, InGaAs, and InAlAs grown by molecular beam epitaxy (MBE). BeO is useful for many applications that require the combined properties of an electrical insulator an excellent heat conductor, with high strength and hardness, with a very high melting point. BeO is frequently used as an insulator base plate in high-power transistors in RF transmitters for telecommunications. BeO is also being studied for use in increasing the thermal conductivity of uranium dioxide nuclear fuel pellets.

The bulk properties of BeO are described in table II below. Sintered BeO, which is very stable, has ceramic characteristics. BeO is used in rocket engines. BeO is used in many high-performance semiconductor parts for applications such as radio equipment because it has good thermal conductivity while also being a good electrical insulator. It is used as filler in some thermal interface materials such as thermal grease. Some power semiconductor devices have used BeO ceramic between the silicon chip and the metal mounting base of the package in order to achieve a lower value of thermal resistance than for a similar construction made with Al_2O_3. It is also used as a structural ceramic for high-performance microwave devices, vacuum tubes, magnetrons, and gas lasers.



Bulk properties of BeO

- Energy bandgap: **10.6eV**
- High thermal stability
- Small bond length (cm^3/mol)
  :BeO(**8.28**) compared to Al_2O_3(**25.8**)
- Well known excellent diffusion barrier
- Dielectric constant: 6.8
- High thermal conductivity (W/m•K)
  :BeO(**300**) compared to Al_2O_3(**35**), Gold (**318**)
- Precursor: **dimethylberyllium**, **$Be(CH_3)_2$**

Table II. Bulk properties of BeO.

1.5 Method to Deposit BeO Thin Film

To grow a thin film of BeO, several physical vapor deposition (PVD) methods including reactive sputtering and E-beam evaporation were attempted but all were unsuccessful due to high diffusivity of Be atoms when their kinetic energy is high. Instead of the physical vapor deposition, having high kinetic energy, a chemical vapor deposition is employed in this study. We report the first chemical vapor deposition route using atomic layer deposition (ALD) to deposit BeO on GaAs. Considering self-cleaning effect on GaAs and ALD precursor properties, a dimethylberyllium, $Be(CH_3)_2$, whose sublimation temperature is 120~130°C at 0.2~0.3 Torr [14], was chosen as a viable BeO precursor. Unfortunately, only two organometallic BeO precursors, beryllium chloride

($BeCl_2$) and beryllium acetylacetonate, (Be(acac), acac = $CH_3COCHCOCH_3$), are commercially available, both of which are not suitable $Be(CH_3)_2$ substitutes for ALD. The high sublimation temperature of $BeCl_2$ (>200^oC) precludes the use of the Cambridge ALD™ system for chemical vapor deposition which is restricted to an upper temperature limit of 200^oC. Subsequently, a $BeCl_2$ pulse could not be observed even if heating was carried out at low pressure (~ 0.2–0.3 Torr). In contrast, Be(acac) has a low sublimation temperature (~ 100^oC), but exhibits insufficient reactivity with water to create BeO in the vapor phase.

1.6 Dimethylberyllium Precursor Synthesis for ALD BeO Deposition

The desired BeO precursor ($Be(CH_3)_2$) was synthesized from $BeCl_2$ via Grignard metathesis [15], and subsequently utilized for the first time as an ALD precursor. Methyl magnesium bromide (CH_3MgBr, 2.5 M in diethyl ether (Et_2O)) was added drop wise over a period of 10 min to a rapidly stirred solution of $BeCl_2$ in anhydrous Et_2O cooled to –30 °C. After stirring the resulting slurry for 12 h, the solvent was removed under reduced pressure. The residual colorless solid was then extracted with benzene and filtered to remove precipitated magnesium salts. Subsequent removal of the residual benzene under reduced pressure afforded $Be(CH_3)_2$ solvated with approximately 2.5 molar equivalents of Et_2O (see Fig 2 for the ^1H NMR spectrum (C_6D_6) of this material). As expected, the protons assigned to the methyl groups of $Be(CH_3)_2$ were strongly shielded ($\delta = -0.45$ ppm) due to the inverse polarity of the Be-CH_3 bonds (Be is more electropositive than C and H). Multiple rounds of sublimation and pre-heating below the sublimation temperature were successful in removing the residual Et_2O which resulted in better purity and improved ALD BeO gate dielectrics on Si and III-V substrates, as for the first time demonstrated below. The precursor synthesis was done by Prof. Bielawski's group at UT in the chemistry department.

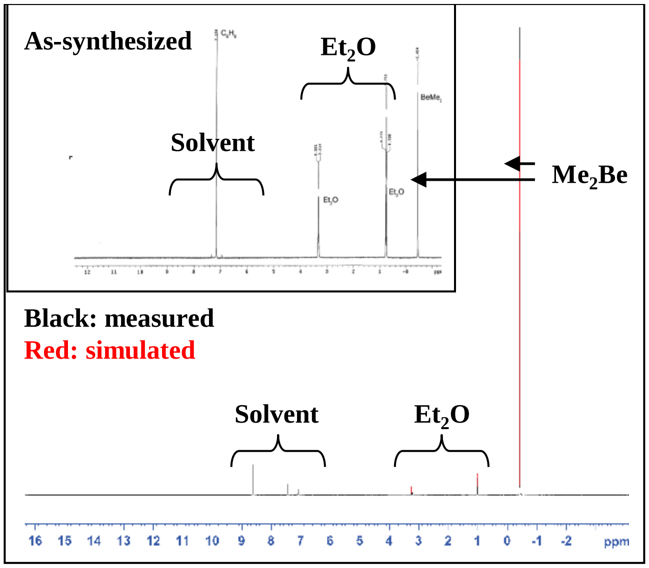


Fig 2. ^{1}H NMR spectrum of dimethylberyllium for Be precursor (C_6D_6).

1.7 Chapter Organization

Overall properties of ALD BeO high-k dielectric materials on channel substrates such as Si, GaAs, and InP in this study are based on understanding of characteristics using physical, optical and electrical analysis, and process development in BeO dielectric MOSCAP and MOSFET characteristics. Chapter 2 covers several fundamental physical and electrical properties to characterize BeO bulk and film using Raman, XPS, AFM, and TEM analysis. Chapter 3 presents more detailed physical characteristics such as the band structure, crystallinity, crystal structure, surface morphology, surface energy, and atomic configuration of ALD BeO. The self-cleaning reaction of BeO precursor, thermal stability and oxygen diffusion characteristics are also covered. Chapter 4, 5, and 6 cover Si, GaAS, InP MOSCAPs and MOSFETs device characterization using ALD BeO gate dielectric. Chapter 7 focuses on the study of density functional theory of $Be(CH_3)_2$ precursor to understand the reaction mechanism and self-cleaning reaction. Chapter 8 evaluates and compares the gate dielectrics such as Al_2O_3, BeO, SiO_2, and HfO_2 using electromagnetics and thermodynamics.

CHAPTER 2: Fundamental Physical and Electrical Analysis

2.1 MOS Device Fabrication

Electrical and physical characterization were performed on MOS capacitors which were fabricated on Si, GaAs and InP substrates each with doping concentrations of around $5 \times 10^{17}/\text{cm}^3$. After HF surface cleaning, 5 ~ 10 nm ALD BeO was deposited at 200^{o}C using a Cambridge Nanotech ALD™ module. BeO was deposited using dimethyl beryllium and water for reagents. For control samples, ALD Al_2O_3 MOS capacitors were also fabricated using trimethyl aluminum (TMA), and water under the same conditions. Physical thickness was measured by ellipsometry with various wavelengths and vertical angles between 45 ~ 75^{o} and confirmed by TEM. Post-deposition annealing (PDA) in the range of 500^{o}C to 600^{o}C was performed by rapid thermal annealing in N_2 ambient for 30 sec – 3 min, followed by the reactively sputtered TaN (2000 Å) as the gate electrode. After patterning and etching, post metal-deposition annealing (PMA) was done at 400^{o}C, 5 min in the forming gas ambient. The leakage current and capacitance were measured using a Keithley semiconductor parameter analyzer and HP4284A LCR meter with frequencies varying from 1 MHz to 1 kHz, respectively. Electrical characterization was performed on MOS capacitors. EOT values were extracted from the capacitance-voltage (C-V) data using the NCSU CVC program.

2.2 Raman Spectrum and X-ray Photoelectron Spectroscopy

Fig. 1(a) shows the Raman spectrum of ALD BeO. There is a significant BeO peak at 1050cm^{-1} (the reported BeO bulk Raman peak, 1084cm^{-1}) [1, 2, 3], compared to

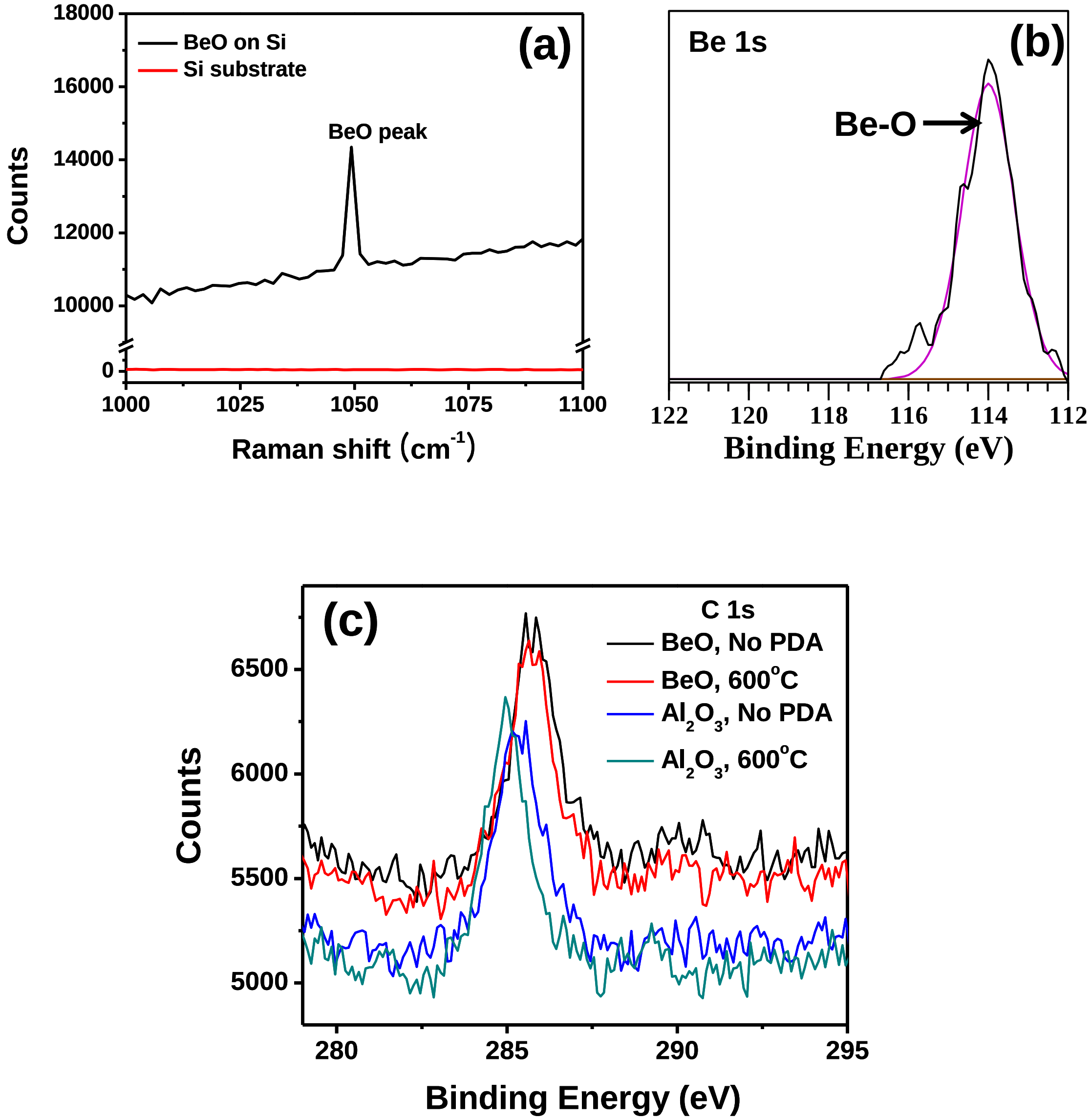


Fig 1 (a) Raman spectrum, (b) XPS of Be 1s, (c) XPS of C 1s.

bare Si substrate, which has no peak in the frequency range between 1000 and 1100cm^{-1}. Fig. 1(b) displays the Be 1s signal between 116 and 112 eV [4]. From these two analyses, we can confirm that ALD BeO is successfully deposited on Si substrates. From Gibb's free energy calculation, there is no possibility of beryllium silicate (Be_2SiO_4) formation [5]. Be 1s XPS shows only BeO formation, not beryllium silicate. Fig 1(c) is C 1s signal, and it shows that ALD BeO has a slightly higher amount of carbon impurities within the dielectric film, compared to ALD Al_2O_3. And the shift of C-H signal at around 285eV between Al_2O_3 and BeO may be related to the atomic network of C and H bonding [4].

2.3 Surface Roughness of ALD BeO thin film

As shown in Fig 2, BeO deposited surface exhibits a relatively low RMS roughness of 0.194 nm. It may be due to the smaller length of the Be-O bond. BeO and Al_2O_3 have molar volumes of 8.28cm^3/mol and 25.81cm^3/mol, respectively [6].

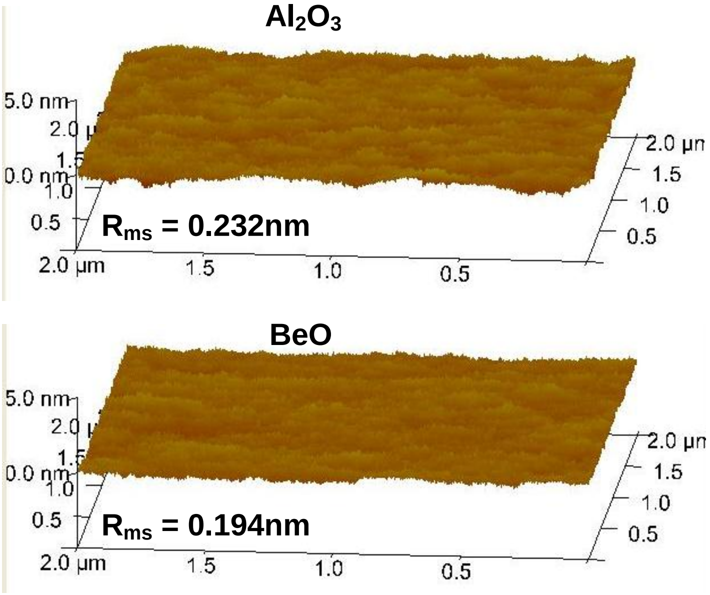


Fig 2. AFM images of 5nm ALD BeO and Al_2O_3 grown on GaAs after HF treatment.

2.4 Transmission Electron Microscopy Analysis

All samples for transmission electron microscopy (TEM) analysis were prepared with the use of a Disco 321 DAT dicing saw, followed by the use of a focused ion beam FIB 200 to achieve an electron transparent thickness.

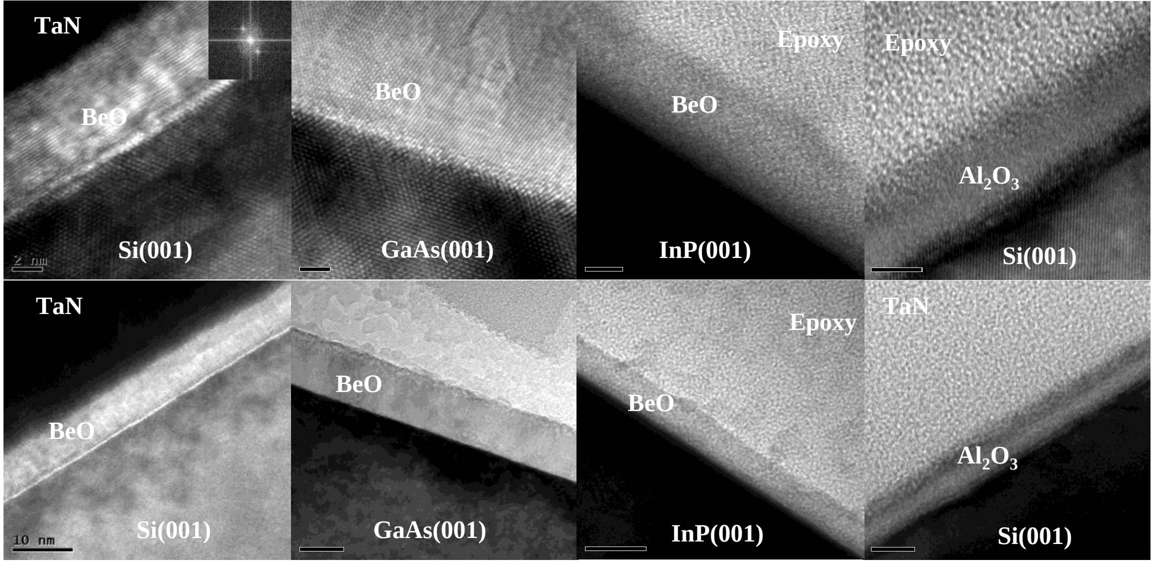


Fig 3. High resolution cross sectional TEM analysis of TaN/BeO/Si, GaAs and InP substrates without PDA.

The high resolution cross sectional TEM analysis for non-annealed BeO on Si and GaAs samples [Fig 3] shows that the ALD BeO thin film was grown on Si and GaAs as a layered crystal regardless of PDA conditions. Fig. 3 shows the near single crystallinity of ALD BeO thin film on Si and GaAs is extended to almost the entire sample, unlike most of the other ALD dielectrics, which tend to have an amorphous or polycrystalline structure with numerous grain boundaries [7]. BeO is expected to exhibit very low crystallization energy due to the small Be atomic size, and results in smaller density of the grain boundaries in the ALD BeO thin film, which is advantageous from the reliability and variability standpoint [8]. However, as-deposited ALD Al_2O_3/Si and BeO/InP is perfectly amorphous and the transition between Al_2O_3 and Si substrate is not relatively sharp compared to that between BeO and Si substrate. The amorphous properties of BeO on InP, unlike other substrates, may be due to the mismatch of atomic spacing or lattice constant on InP.

2.5 Electrical Characteristics for MOS Capacitors

Fig. 4(a) shows the physical thickness versus EOT, which allows extracting the dielectric constant. Fig 4(b) also displays the frequency dispersion plot, in the range of 1 MHz ~ 1 kHz, as well as the hysteresis, Fig. 4(c), in TaN/BeO/Si MOS capacitors. The dielectric constants of the BeO film are k = 6.5 before annealing and k = 6.8 after annealing. For comparison, the Al_2O_3 dielectric constant changes significantly by annealing, from k = 6.4 to 7.2. Such difference may be related to the thermal stability of the atomic networks of BeO and Al_2O_3. BeO is already crystallized as grown and therefore, its local structural characteristics don’t change much after annealing. ALD BeO shows negligible frequency dispersion and hysteresis in Fig. 4(b) and (c). Fig. 5 shows the distribution of the V_{fb} values of the Al_2O_3 and BeO MOS capacitors fabricated using the 50, 65 and 80 ALD cycles. ALD BeO is observed to exhibit lower V_{fb} variability.

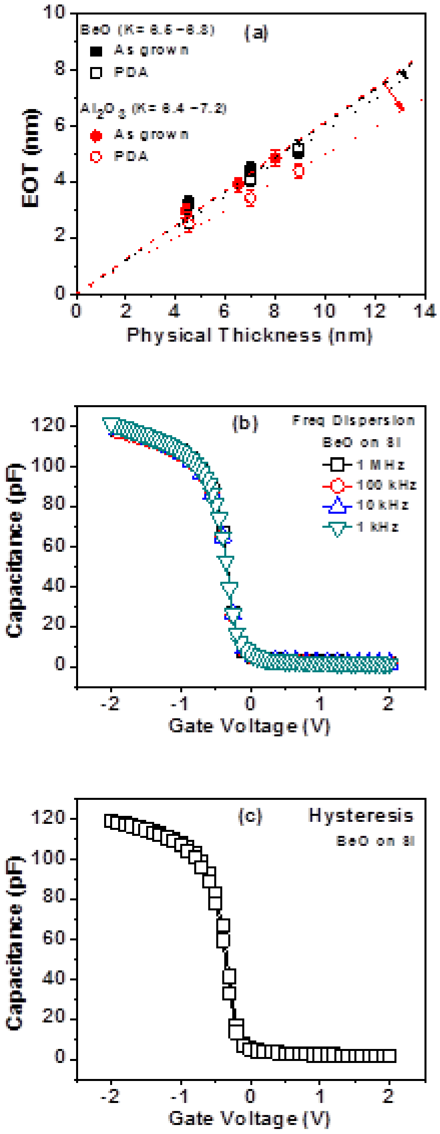


Fig 4. (a) Physical thickness versus EOT without/with PDA, (b) Frequency dispersion and (c) Hysteresis. Frequency dispersion is measured capacitances with frequencies between 1MHz and 1KHz. Hysteresis is voltage sweep up and down.

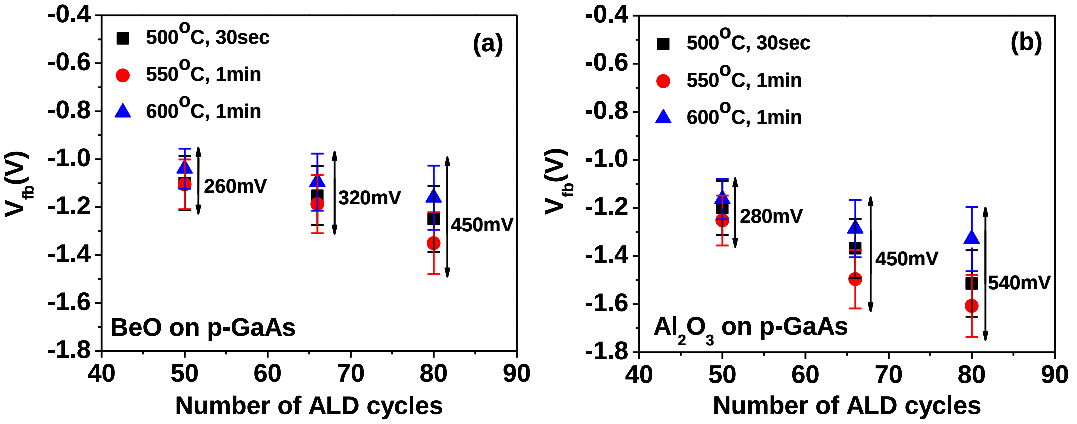


Fig 5 Statistical V_{fb} variability of (a) BeO and (b) Al_2O_3 respectively, with several PDA conditions.

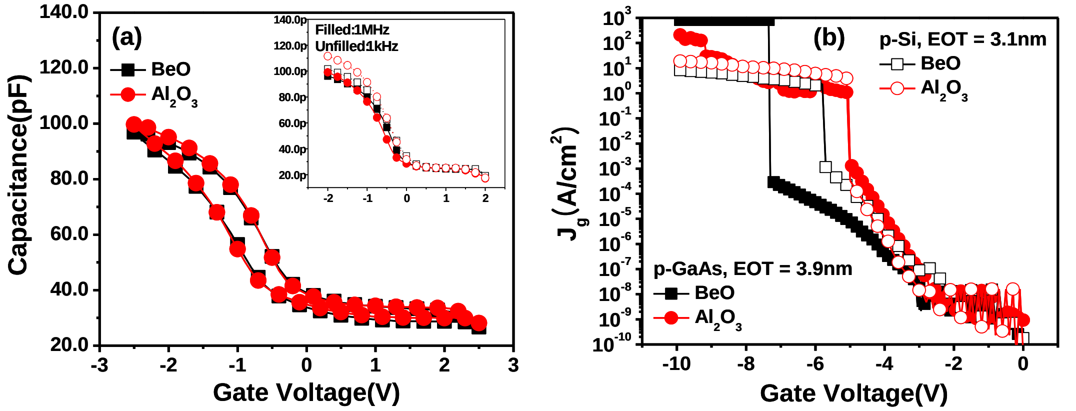


Fig 6. (a) C-V and (b) I-V characteristics of BeO and Al_2O_3 on p-GaAs(100) substrate with ~ 3.9nm EOT. Inset of (a) shows frequency dispersion at 1MHz and 1kHz for each oxide.

Fig 6 shows the C-V characteristics of the MOS capacitors with 3.9 nm EOT of Al_2O_3 and BeO on GaAs substrates. The inset demonstrates the frequency dispersion between 1 MHz and 1 kHz. The leakage current density vs. gate voltage for the same device is shown in Fig 6(b). ALD BeO on Si displays the similar leakage current compared to that for ALD Al_2O_3. However, ALD BeO on GaAs shows lower leakage current and significant higher breakdown voltage, unlike Si substrate. As expected, at high electric fields, BeO exhibits lower leakage current than Al_2O_3 due to its larger energy band gap [9].

CHAPTER 3: Advanced Physical Analysis of ALD BeO Film

3.1 Band structure Determination

Oxygen vacancy is the dominant origin of conduction band offset (ΔE_c) and energy bandgap (E_g) lowering for bulk and thin films, and it may facilitate the diffusion of oxygen [1]. Therefore, the study of ΔE_c and E_g may offer an insight about oxygen diffusion [1, 2]. The ΔE_c of ALD BeO thin film is still not explicitly known even though ab initio calculations of E_g and ΔE_c were performed in a previous study [3, 4]. Fig. 1(a) is the vacuum ultra-violet (VuV) spectroscopic ellipsometry results of the BeO (Al_2O_3) film on the p-Si substrate for full energy band-gap analysis [5]. For available data in Fig 1(a), we can estimate BeO E_g to be 7.87 ~ 7.91eV. However, E_g determination is based on the linear extrapolation of absorption for photon energy, much greater than E_g (we don't have access to that spectral region), causing uncertainty in exact E_g determination. (*The results in Fig 1 require more investigation*). Fig. 1(b) shows the SHG results, done in Prof Downer's lab, for the 5 nm BeO (Al_2O_3) film on the p-Si substrate. Since the transition from three photon to two photon processes take place at around 1.67eV and 1.71eV before and after PDA, respectively, one can estimate the BeO ΔE_c with Si substrate to be of 2×1.67eV(1.71eV) – 1.1eV (Si energy band gap) = 2.24eV and 2.32eV, before and after PDA, respectively. Although it is not possible to do a similar SHG study on GaAs because it is not a centro-symmetric material like Si, one may expect, based on the Anderson affinity rule, a conduction band offset between BeO and GaAs to be higher than that of Al_2O_3 in III-V. Also, internal photoemission (IPE) analysis can provide the further evident information about the interface characteristics (including ΔE_c) of ALD BeO gate stack. ALD BeO displays the relatively low photocurrent compared to Al_2O_3 in

Fig 1(c). T The lines indicate the linear interpolation procedure used to infer the electron energy barrier Φ_e. he amorphous nature of the insulator results in a significant subthreshold IPE, indicative of oxide CB tailing [6]. And there is the same value of the fundamental IPE threshold as in the both crystalline and amorphous cases due to no significant influence of the momentum conservation condition [6]. Therefore, extraction of the IPE threshold from $Y^{1/p} - h\upsilon$ plots of crystalline BeO is a valid procedure of interface barrier determination. From IPE analysis in Fig 1(c), one can infer that ALD BeO has 0.4eV higher ΔE_c compared to that for ALD Al_2O_3. The reported Al_2O_3 ΔE_c is around 1.9eV [7]. Thus, ALD BeO ΔE_c may be around 2.3eV. These results match fairly with IPE results ($\Delta E_c = 2.3$eV) in Fig 1(b).

Figure 2 shows the synchrotron XPS spectra of the BeO VB region. To correct for instability in the synchrotron beam energy over time, each VB spectra was simultaneously measured, then aligned, with the Si $2p_{3/2}$ core level (binding energy = 99.42 eV). The zero of energy of Fig. 2 is referenced to the mid-gap of the silicon substrate. The VB edge is obtained by linear extrapolation of the absorption onset and found to be 4.7 *eV* below the mid-gap of Si, which yields VBO = 4.14 ± 0.2 *eV*. Fig. 3 illustrates the band diagram of (a) HfO_2, (b) HfO_2/ Al_2O_3 and (c) HfO_2/BeO IPL MOSCAPs. BeO band structure was estimated from previous analysis. From optical measurements, the band offsets (ΔE_c and ΔE_v) of BeO with Si are much larger than those of Al_2O_3 or HfO_2.

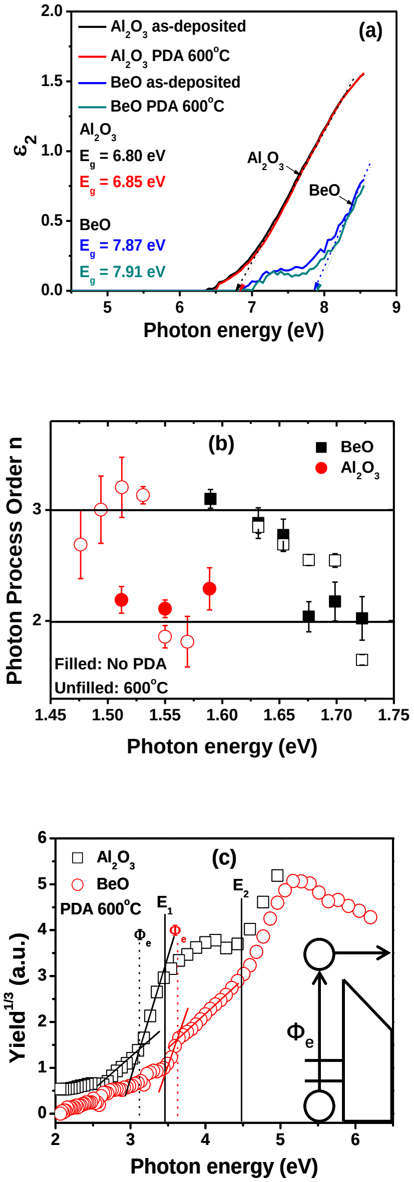


Fig 1. (a) VuV spectroscopic ellipsometry results for full energy band-gap analysis. (b) SHG results of BeO(47.8 A) and Al_2O_3 (48.5 A) on p-Si(100). (c) Spectra of electron IPE from the VB of silicon to the CB (cf. the insert) of crystalline BeO epitaxially grown on (100) Si as compared to amorphous film of Al_2O_3 on (100) Si, linearized in $Y^{1/3}$ – hυ coordinates.

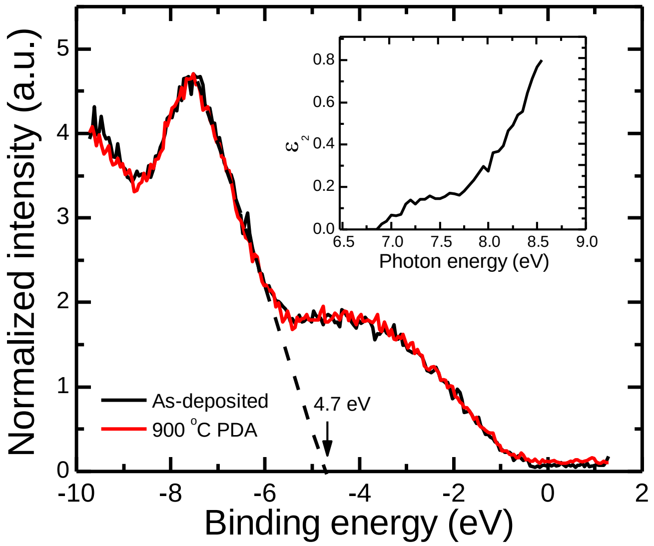


Fig. 2. (Color online) XPS spectra of BeO VB structure and the inset on the right top corner shows the absorption spectra of as-deposited sample measured by SE.

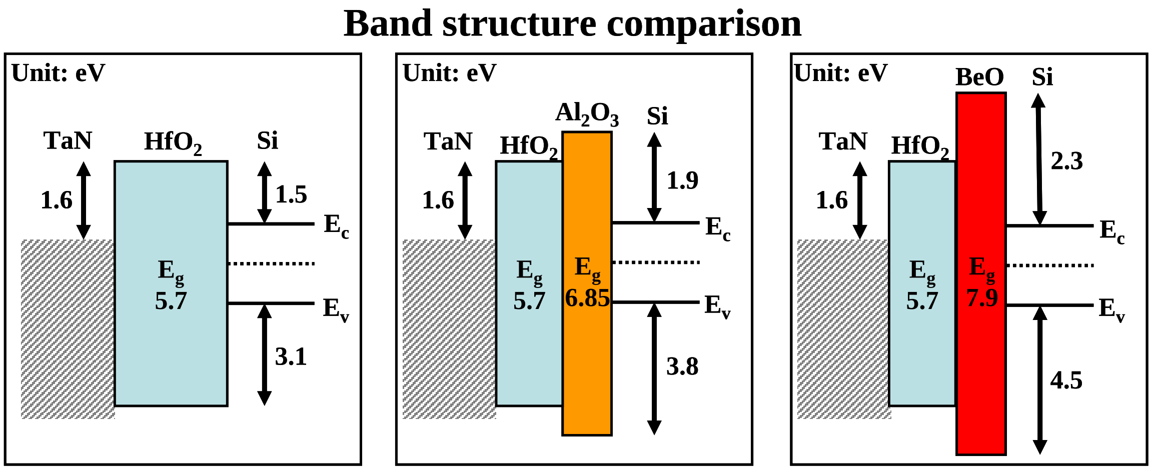


Fig 3. The schematic band structures of HfO_2, HfO_2/Al_2O_3(IPL) and HfO_2/BeO(IPL) gate stacks on Si substrate. ALD BeO band structure was estimated from analysis of data in Fig 1.

3.2 Crystal Structure and Surface Morphology of BeO Film

Fig. 4 shows a typical 2θ scan of BeO layer (24nm thickness) grown on a Si(100) substrate. Besides the Si peak at 2θ = 69^o, there is only one main peak of BeO at 2θ = 43.3^o in a wide range scan. It is (101) peak of the wurtzite crystal and coincides with the TEM d-spacing result. The tiny shift of BeO (101) peak may be due to the strain or stress, or tilt with some uncertainty. The small peak at 50.5^o is close to the BeO zinc-blend [200] 2θ = 47.9^o. The single crystalline domain structure of ALD BeO thin film grown on Si(100) is further confirmed by the electron diffraction pattern from plane view samples.

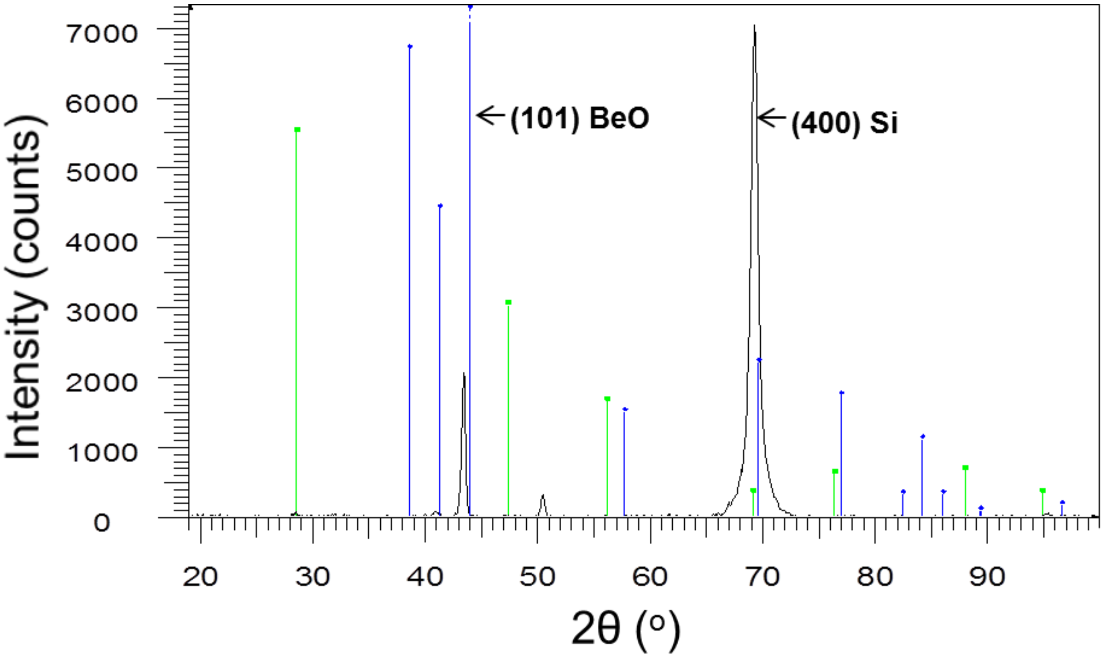


Fig 4. XRD 2θ scan of BeO (24nm) layer grown on a Si(001) substrate. There is one significant peak of BeO at 2θ = 43.3^o. It is the [101] wurtzite plane.

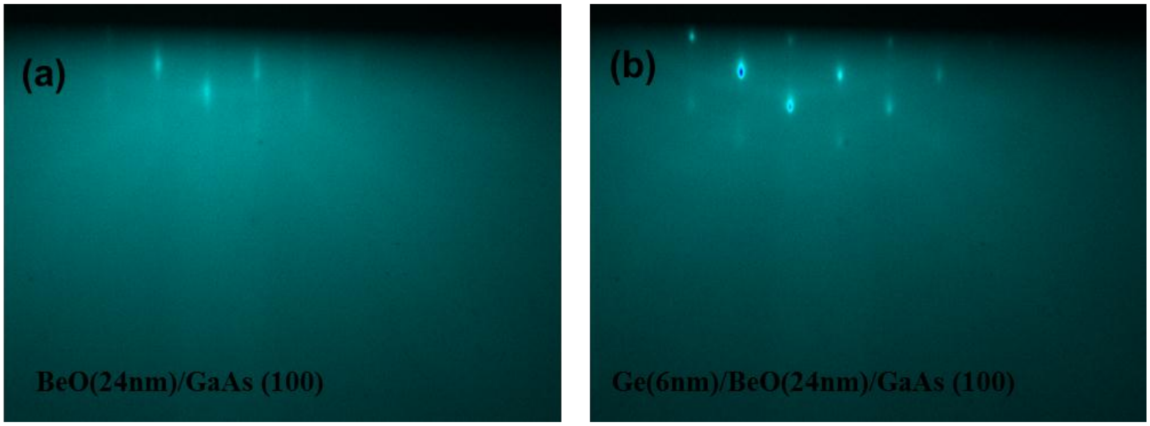


Fig 5. RHEED image of (a) ALD BeO on GaAs, and (b) Ge epi grown on BeO.

Reflection high-energy electron diffraction (RHEED) is a technique used to characterize the surface of crystalline materials. RHEED systems gather information only from the surface layer of the sample, which distinguishes RHEED from other materials characterization methods that also rely on diffraction of high-energy electrons. In the RHEED setup, only atoms at the sample surface contribute to the RHEED pattern. The glancing angle of incident electrons prevents them from escaping the bulk of the sample and reaching the detector. Atoms at the sample surface diffract (scatter) the incident electrons due to the wavelike properties of electrons. The diffracted electrons interfere constructively at specific angles according to the crystal structure and spacing of the atoms at the sample surface and the wavelength of the incident electrons. Some of the electron waves created by constructive interference collide with the detector, creating specific diffraction patterns according to the surface features of the sample. Users characterize the crystallography of the sample surface through analysis of the diffraction patterns [8, 9]. Figure 5 shows a RHEED pattern of ALD BeO (24 nm) on GaAs substrate. The measurement conditions are that glancing angle of 4 degree, 18 keV electron energy, filament current of 1.5A, and beam current of ~ 0.2 µA. From this image, one can infer that the surface of ALD BeO on GaAs is quite smooth and it is close to single crystal with hexagonal surface structure. The high crystallinity of ALD BeO may be related to its large grain size. When a MBE Ge (6 nm) epitaxial layer was grown on a BeO (24 nm) surface, the Ge epitaxial layer is likewise highly crystalline.

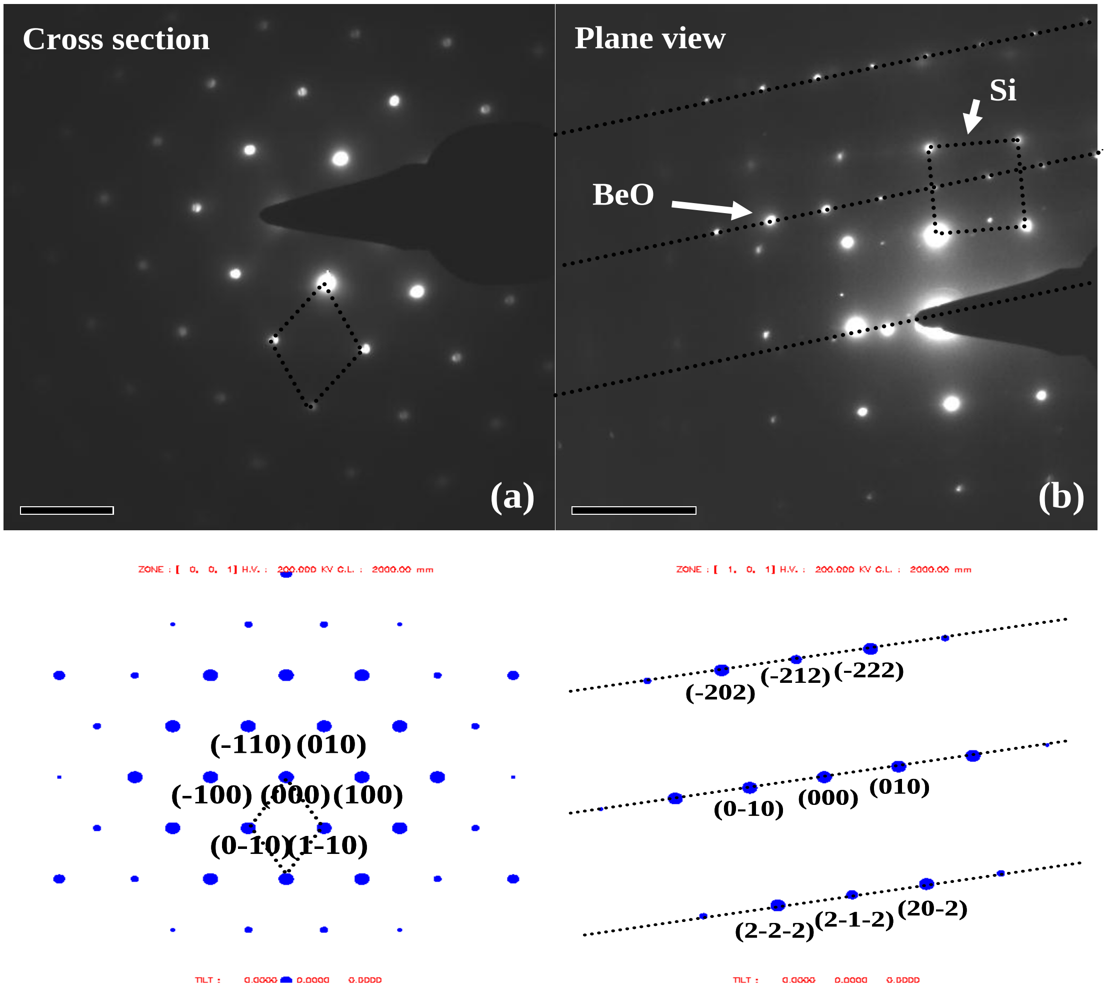


Fig 6. (a) Cross sectional SAD and (b) Plane view SAD for the as-deposited ALD BeO film. (c) SAD simulation pattern of (c) (001) and (d) (101) wurtzite BeO crystal plane.

Figs. 6 (a) and (b) show the cross sectional and plane views SAD, respectively, for the as-deposited ALD BeO film. In Fig. 6(a), the SAD pattern from (001) cross section specimens was obtained using a large aperture that covered BeO layer with some silicon substrate contribution. The cross sectional SAD in Fig. 6(a) contains only Si diffraction spots. One can expect that BeO diffraction spots may be parallel and overlapped with Si diffraction spots. In fact, the lattice constant of bulk wurtzite BeO is a=b=2.7 Å and c=4.3 Å, and it is exactly one half of Si (diamond structure) lattice constant (a=b=c=5.4 Å). The hexagonal BeO lattice can be matched nearly perfectly to the Si(001) plane due to symmetry and atomic spacing [Fig 6(b)], which allows an epitaxial growth. It also opens up the possibility of epitaxial Si overgrowth on the BeO, leading to SOI. The plane view SAD in Fig. 5(b) shows both Si and BeO diffraction spots corresponding to [101] orientation of wurtzite structure. The SAD simulated patterns of (001) and (101) wurtzite BeO [Fig. 6(c) and 6(d), respectively] are well matched with the experimental results shown in Fig. 6(a) and (b), respectively. It clearly shows that ALD BeO was grown epitaxially hexagonal-on-cube. The SAD patterns from other locations were identical to this one, indicating ALD BeO film is crystallized over a large area.

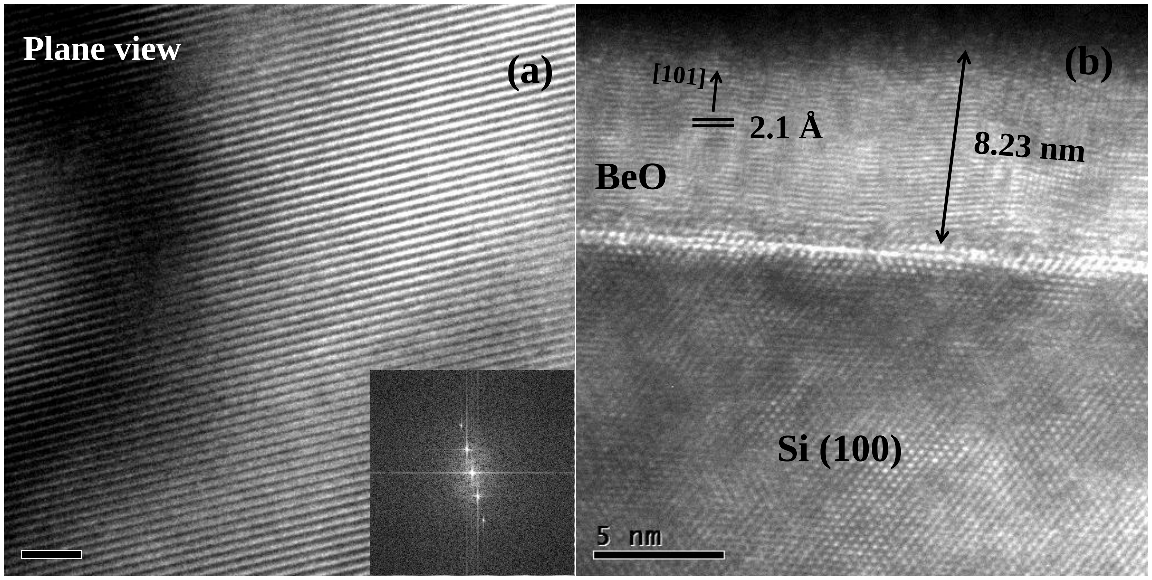


Fig 7. High resolution plane view (a) and cross sectional (b) TEM analysis of BeO/Si stacks without PDA. The in-set, diffractogram is obtained from Fast Fourier Transform (FFT).

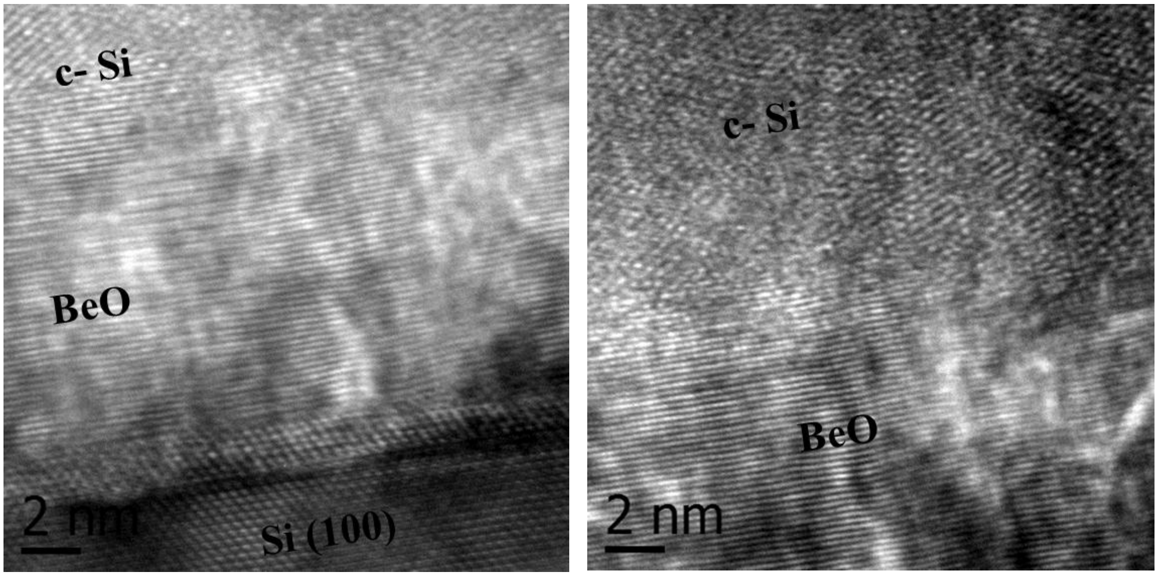


Fig 8. Cross sectional TEM images of CVD grown Si epi layer on BeO/Si substrate.

Fig. 7 shows the well-ordered crystal structure of the ALD BeO layer in high resolution plane view TEM without and with PDA. The in-set diffractogram which is obtained from the Fast Fourier transform (FFT) processing, in Fig. 7(a) also well supports the crystallinity of ALD BeO. One observes some dark surface regions of BeO crystal in Fig. 7(a). It may be due to the thickness variation of the thin foil with some uncertainty. ALD BeO thin film was grown as a layered single crystal without significant grain boundaries. The distance between layered BeO lattices, called d-spacing, is around 2.1Å, which is close to (hkl) = (101) plane of wurtzite structure from a powder diffraction pattern database. The crystal structure of bulk BeO is wurtzite. An atomically sharp transition from the crystalline Si substrate to the layered crystalline BeO can be seen in the HRTEM images. No significant interfacial layer can be distinctly observed between the Si substrate and the BeO layer with and without PDA. Si epi layer grown on the BeO/Si(substrate) shows high crystallinity in Fig 8. The BeO structure is also particularly useful as a substrate for hetero-epitaxially growing diamond-type structures [10]. Thus, Si, SiGe, or Ge channel materials, which have the same crystal structure as diamond, can be grown on BeO dielectric for SOI technology.

3.3 BeO Atomic Structure and its Surface Energy

From above analysis, we conclude ALD BeO is close to the layered single crystal of wurtzite structure with [101] orientation. Hereby, the atomic structure of ALD BeO is constructed based on the above analysis. Fig. 9 shows the constructed wurtzite crystal structure of BeO using “diamond” (the name of software) simulation software. Based on the above results, (101) plane shown in Fig. 9(a) is interpolated in wurtzite BeO crystal structure, and the constructed wurtzite crystal in Fig. 9(b) is slightly rotated to observe the atomic network readily with (101) plane shown distinctly. In Fig. 9(b), the atomic spacing between Be atoms A and B (A and C) is 2.7Å (3.8Å). It is exactly matched with the atomic spacing of Si unit cell (diamond Si: a/2=2.7Å, fcc Si: a=3.8Å). And one can expect that BeO surface is Be or O terminated [Fig 7]. ALD BeO deposition cycle is terminated with a water pulse. Therefore, ALD BeO surface may be only oxygen terminated, and it may lower the surface energy and improve the interface quality between BeO and gate electrode.

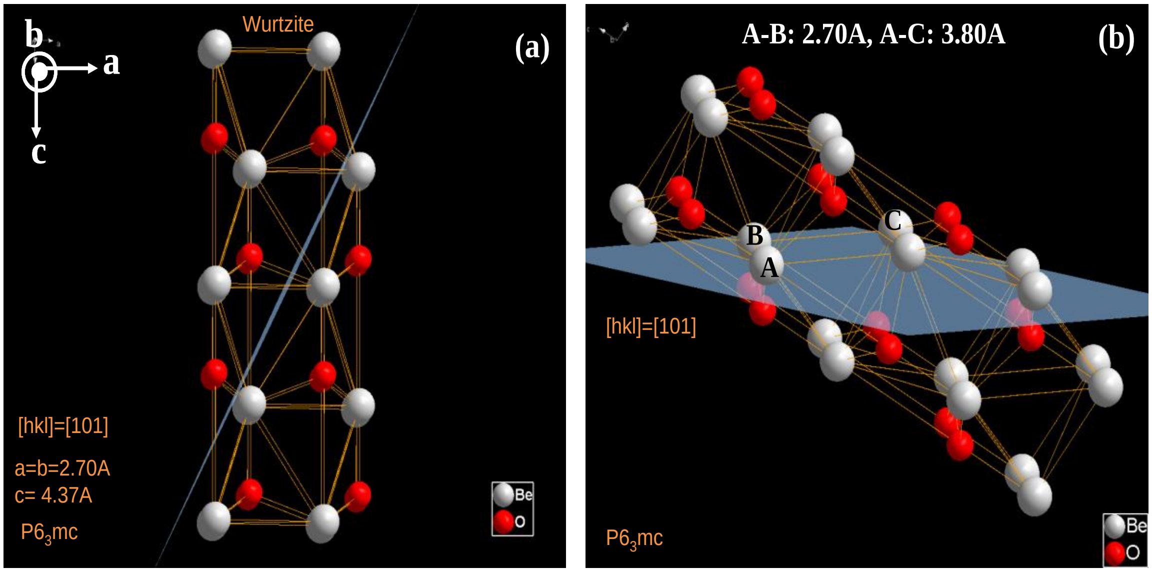
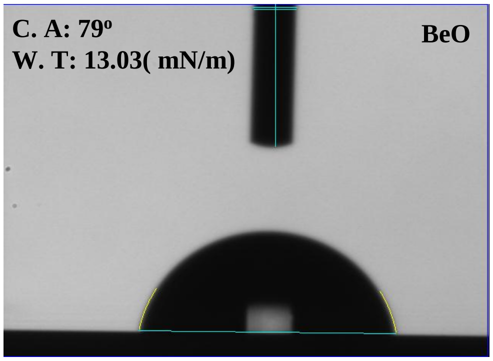


Fig 9. Diagram of wurtzite BeO crystal structure using “Diamond” simulation software. Wurtzite BeO (101) plane in Fig 9(a) is interpolated in crystal structure. Fig 7(b) is the rotation of Fig 7(a) to observe the atomic network with (101) plane distinctly.

The surface energy between Al_2O_3 and BeO layers was compared approximately using contact angle measurement [11, 12]. Fig 10(a) is the contact angle measurement and DI water is used as a liquid drop. The contact angle (C.A) and wetting tension (W.T) of BeO (Al_2O_3) are 79^{o} (83^{o}) and 13.03 (8.6) mN/m, respectively. From Fig 10, one can infer that BeO may have lower surface energy than Al_2O_3. The BeO molecules are more strongly bound to the substrate than to each other. The first complete monolayer is then covered with a somewhat less tightly bound second layer. As the layered films grow, the decrease in bonding energy is continuous toward the bulk crystal value. Single crystal epitaxial growth of semiconductor films is the most important example of this growth mode.



	Contact angle	**Wetting tension(mN/m)**
Al_2O_3	**83^{o}**	**8.60**
BeO	**79^{o}**	**13.03**

Fig 10. Contact angle measurement, and DI water is used as a liquid drop. The contact angle (C.A) and wetting tension (W.T) of BeO (Al_2O_3) are 79^{o} (83^{o}) and 13.03 (8.6) mN/m, respectively.

3.4 Self-cleaning Reaction and Oxygen Diffusion Barrier

Ex situ X-ray photoelectron spectroscopy (XPS) analysis was performed in a UHV chamber equipped with a monochromatic Al K_α X-ray source. Fig 11 shows the Be

1s and Al 2p XPS analysis for 15Å BeO and Al_2O_3 samples, respectively. ALD Al_2O_3 is efficient and better known diffusion barrier layer than HfO_2 [14]. Accordingly, Al_2O_3 was studied to compare the performance between BeO and Al_2O_3 in the view point of oxygen diffusion barrier.

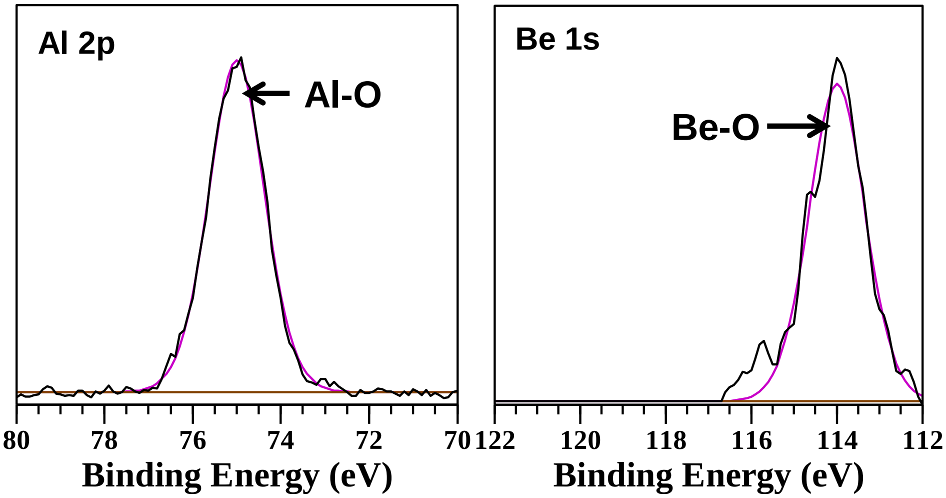


Fig 11. XPS spectra for Be 1s and Al 2p of 15 Å (a) Al_2O_3 and (b) BeO gate stacks.

The binding energies of Al_2O_3 2p and BeO 1s are 74 ~ 76 eV and 112 ~ 116 eV, respectively as shown in Fig 11. The outermost valence band electrons, related to the atomic cohesion, of Al_2O_3 and BeO are Al 3p and Be 2s, respectively. Therefore, one can infer that the binding energy of Be-O is some higher than that of Al-O. As bond distance decreases, binding energy increases, and it leads to the high melting point of BeO (2507 ^{o}C) compared to Al_2O_3 (2072 ^{o}C) [15]. Both BeO and Al_2O_3 are almost covalent bonding [16]. And the short bond distance leads to more orbital splitting and results in the high energy band gap [17]. The high energy band gap stands for the suppression of the oxygen vacancy [1, 2]. Hence, one can infer that BeO may be the efficient oxygen diffusion barrier even there are still many factors such as atomic networks. After 900 ^{o}C PDA in

Fig 12, ALD BeO shows the 32 % reduced Si-O peak compared to Al-O peak. These experimental results well support the theoretical basis.

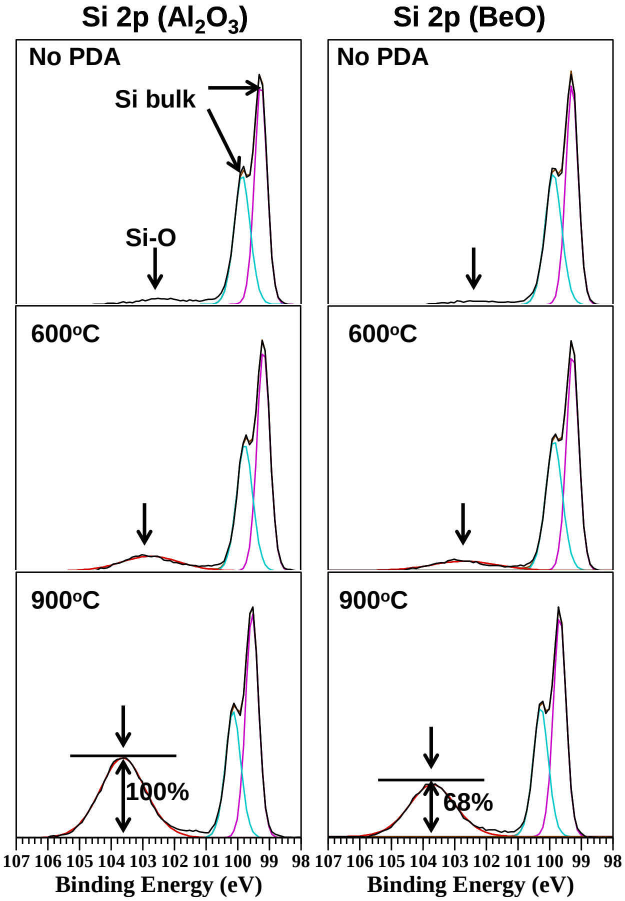


Fig 12. XPS spectra for Si 2p of 15Å (a) Al_2O_3 and (b) BeO gate stacks. Interfacial layer (Si-O peak) increases with PDA temperature increase. However, BeO displays 32% less interfacial native oxide signal compared to Al_2O_3.

Fig. 13 shows the Ga 2p spectra of ZrO_2, Al_2O_3 and BeO deposited directly on GaAs at ALD growth temperature of 250°C. After ALD BeO and Al_2O_3 deposition, both show the reduction of native gallium oxides such as Ga_2O_3 and Ga_2O, at the binding energies of 118.5 ~ 1119 eV and 1118 ~ 1117.5 eV, respectively [18]. ALD BeO shows around 50% lower native gallium oxide signal without PDA and it is still 50% lower after PDA than that for Al_2O_3. However, ZrO_2 shows no self-cleaning reaction, and much increased Ga-O signal after PDA, unlike the other two dielectrics. For the XPS of as-cleaned sample, PDA slightly increases the native gallium oxide signal. It was reported that oxygen transportation from As-O to Ga-O reduces the As-O signal and increases the Ga-O signal during PDA [19].

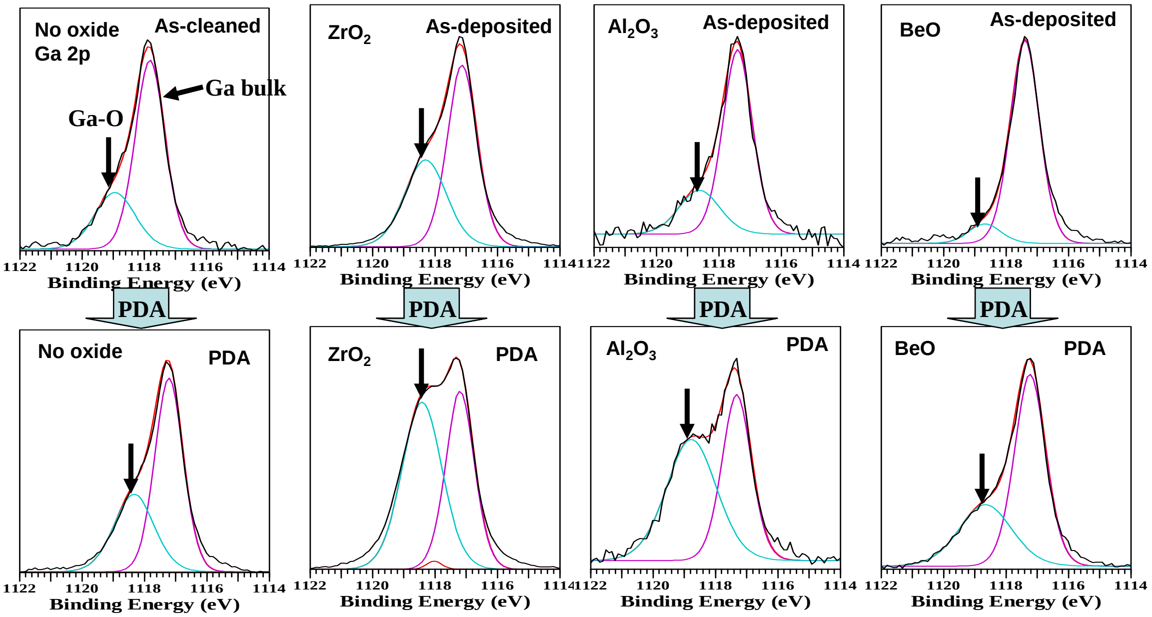


Fig 13. High resolution XPS results of Ga 2p for as-cleaned, ZrO_2, Al_2O_3 and BeO directly deposited on GaAs substrate without/with PDA in N_2.

Fig 14 shows the As 3d spectra of Al_2O_3 and BeO [19]. Both oxides show significant interfacial As-O reduction at the binding energies of 44 ~ 45 eV and after PDA, still no more As-O increase. Above XPS results were repeated in a couple of times

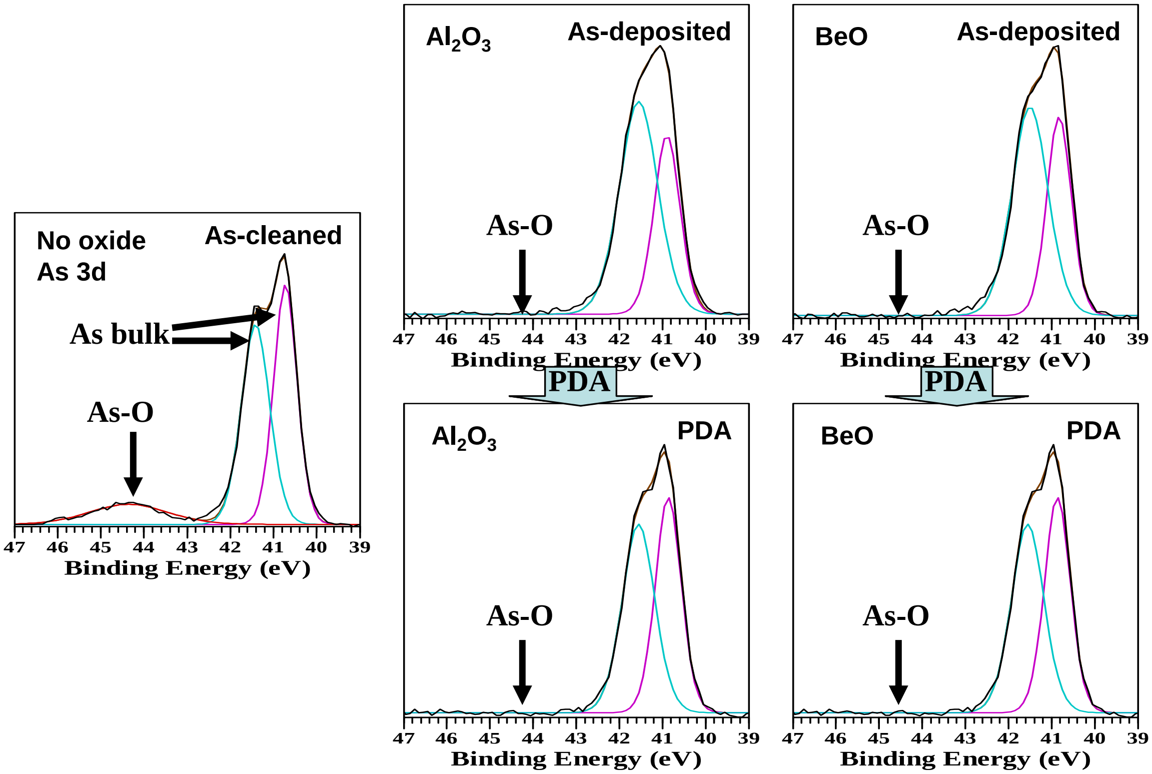


Fig 14. XPS results of As 3d for as-cleaned, Al_2O_3 and BeO without/with PDA in N_2

and the similar trends of Ga 2p, In 3d and As 3d were obtained on InGaAs and InP samples. Therefore, one can infer that the growth of Ga-O during PDA is mainly due to the oxygen from high-k dielectrics and partially from native As-O. Gallium may absorb oxygen actively during PDA and generate oxygen vacancies in high-k dielectric. Beryllium precursor, dimethylberyllium $Be(CH_3)_2$, has two methyl ligands but Al precursor, trimethylaluminum $Al(CH_3)_3$, has three. Due to one less methyl ligand and smaller Be atomic size, the molecular size of Be precursor should be smaller than that of Al precursor. Therefore, Be precursor efficiently absorbs oxygen from the GaAs native oxide, possibly because the number of Be precursor molecules per unit area that adhere to the surface may be larger than in the case of the Al precursor (steric hindrance). And the high bond strength and small atomic spacing between Be and O atoms possibly protects the BeO/GaAs interface from the diffusion of oxygen efficiently. Fig 15 shows the In 3d spectra of Al_2O_3 and BeO. We can expect that BeO precursor has efficient self-cleaning effect compared to Al precursor (trimethylaluminum) due to the less steric hindrance. And also, BeO efficiently prohibits the diffusion of oxygen in Fig 15.

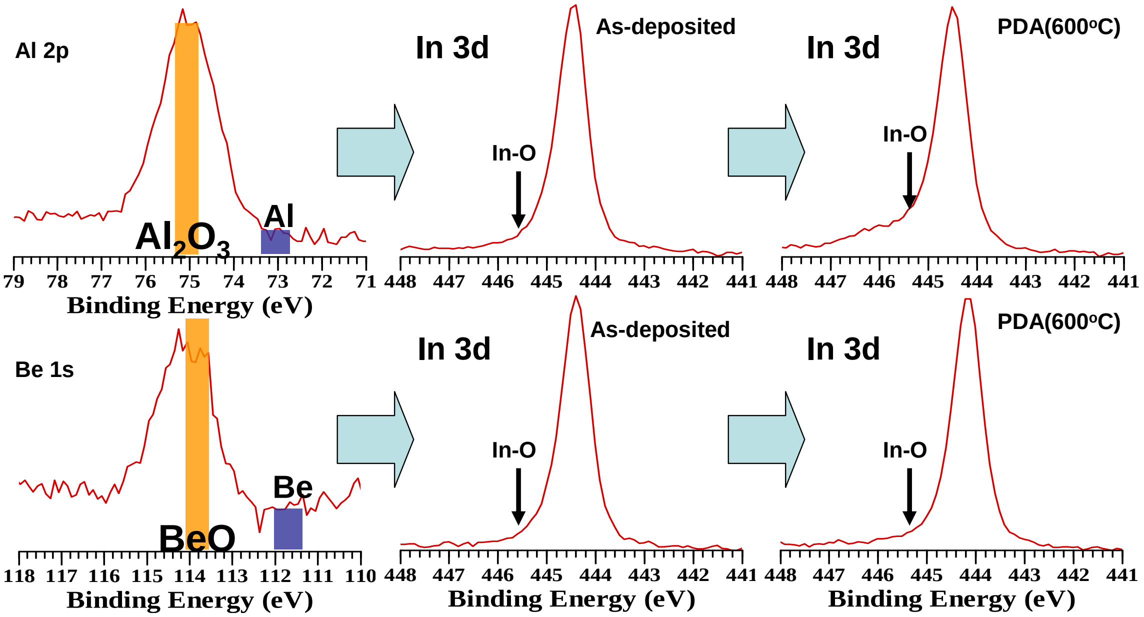


Fig 15. XPS results of In 3d for Al_2O_3 and BeO without/with PDA in N_2

3.5 Nanostructure and interface Characterization of ALD BeO Film

The nanostructure of BeO thin film was not studied experimentally due to the absence of an application for BeO thin film and the difficulties inherent in the evaporation method (the only method to grow BeO before ALD) which requires high thermal energy [20]. BeO possesses a unique combination of thermal, dielectric, and mechanical properties that are highly desirable in electronic applications [15].

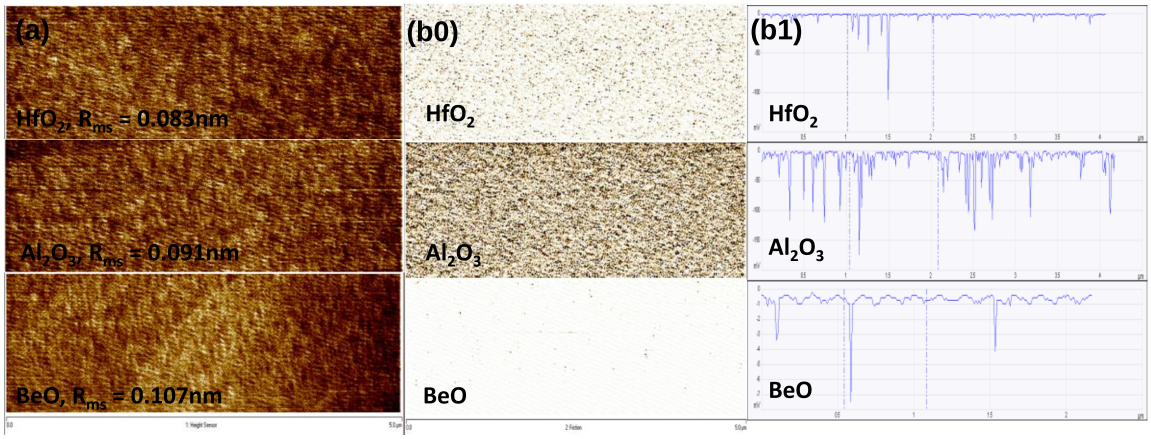


Fig 16. Surface roughness (a), and current spots (b0) and line scan (b1) images at a 1 V backside bias for HfO_2, Al_2O_3, and BeO samples (all 5 Å physical thickness with a scan area 5 × 2.5 μm^2) (b0) BeO displays fewer current leakage spots than the other oxides.

Conductive atomic force microscopy (C-AFM) is especially helpful for investigating semiconductor nanostructures, as well characterizing dielectric layers locally [21, 22]. Unlike traditional techniques that provide spatially averaged information of the microscopic phenomenon, C-AFM allows the dielectric film to be characterized both topographically and electrically with nanometer resolution. Using constant bias and contact modes, we have mapped a few cursory current images. Fig 16 shows C-AFM results on all 5 Å BeO, Al_2O_3, and HfO_2 samples. The physical thickness is calculated from the deposition rate. A backside (or substrate) voltage bias of 1 V was applied, and leakage current was monitored with a sensitivity of 10 nA/V. Fig 16(a) shows that the topography of the image is smooth without any bumps or hollow surfaces. However, the current images in Fig 16(b) display some isolated dark spots, suggesting current conduction through leakage paths [23]. The dark spots in the current image may be due to the low level leakage current under a high electric field, generally known as stress-induced leakage current (SILC) [24]. High crystallinity and band offsets in Figs 1 and 2 may suppress the leakage current and defect generation, resulting in few ALD BeO conduction paths (dark spots). Similar results, displaying many dark spots, were seen in the Al_2O_3 current image. (*To explain this phenomenon, an intensive investigation for C-AFM is required*). To study thermal stability and inter-diffusion at the interface between BeO and the Si substrate during 750 °C annealing, electron energy loss spectroscopy (EELS) analysis was performed (Fig. 17). The EELS results show no detectable inter-diffusion between Si and BeO.

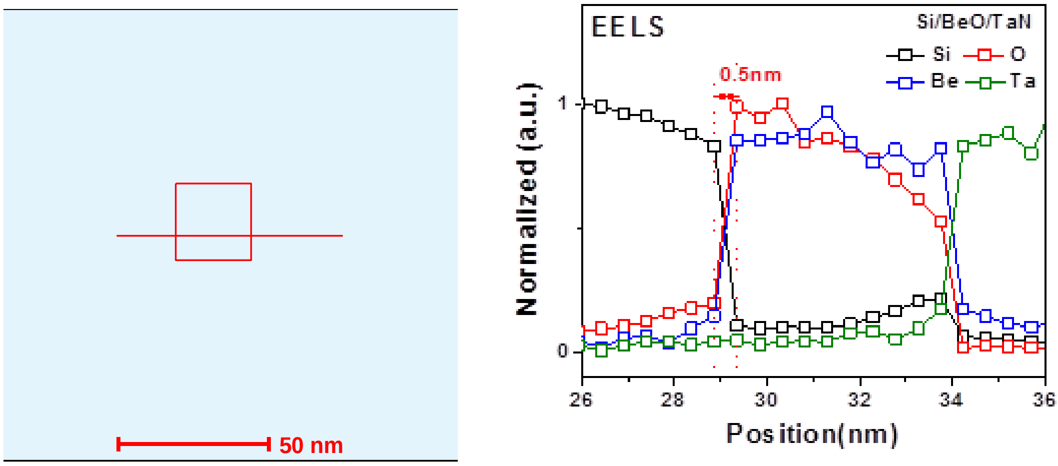


Fig 17. EELS line scan profile for Si/BeO/TaN stacks with PDA at 750 ^{o}C.

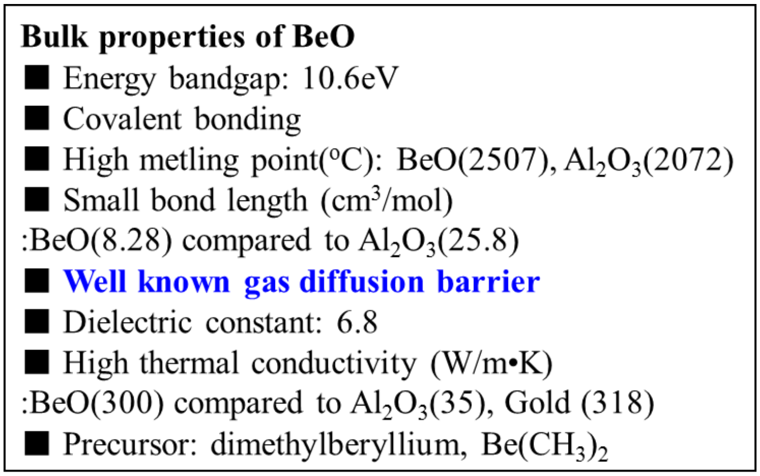
3.6 Oxygen Diffusion and Anti-Corrosion Characteristics

Gas diffusion and anti-corrosion properties of thin film coatings have been under investigated by a number of researchers for application in mechanical parts, packaging, and thin film encapsulation [25-27]. A dense, defect-free and fully covered thin film coating of an inorganic material may effectively render oxidizing gases impermeable.

Unfortunately, most thin films have pinholes and defects caused by the intrinsic/extrinsic stacking faults and the deposition process or substrate imperfections can compromise the gas diffusion barrier properties. Grain boundaries in a barrier film can also be a pathway for high permeation. Recent studies have recommended a multilayer structure as the only practical way to achieve superior diffusion barrier performance [25, 29]. For example, complex multilayer barrier films consisting of six to twelve pairs of polymer and inorganic layers currently approach the performance needed by packaging [28]. However, more recent detailed measurements and modeling of these multilayer structures attribute the “apparent” low transmission rate for these multilayers to long lag times and not to reduction in steady state permeability [29, 30]. This recent study also highlights the need to deposit more perfect single-layer barrier films. Not surprisingly, the deposition process has a significant influence on barrier properties of thin inorganic films [27].

Atomic layer deposition (ALD) is a process known for growing thin, smooth, conformal, pinhole-free films with featureless microstructure and low stress [31]. The particular properties of the ALD process makes it an ideal candidate method to manufacture conformal sealing coatings on precision metallic/organic parts sensitive to corrosion or oxidation. The well controlled surface reactions are expected to diminish the pinhole density enabling sealing even with thin coatings of nanometer thicknesses. At the same time the entire surface is equally coated, avoiding shadowing effects and, as a result, the influence of surface roughness of the substrate is minimized [32, 33]. Thermal ALD has been employed as a method for depositing metal oxide layers onto stainless steel [34–36], metal alloys [37] and organic polymer, which improved the resistance to oxidation or corrosion in H_2O, O_2, acidic, neutral and alkaline solutions. Moreover, plasma-enhanced ALD [38, 39] is an alternative for the coating of heat-sensitive engineering alloys for corrosion protection even at room temperature [40]. The excellent properties of ALD films resulting from sequential, self-limiting surface reactions should produce films that are effective gas diffusion or anti-corrosion barriers. ALD single or multilayer of Al_2O_3 film on polymers has been investigated as an inorganic gas diffusion barrier popularly. However, ALD Al_2O_3 film still has high density of pinholes and defects. As a result, thick ALD Al_2O_3 is required to satisfy the requirement for application. However, thick thickness of ALD Al_2O_3 significantly degrades device performance and process time. Therefore, thinner film coating is preferred to improve the device performance and process time.

To prevent the H_2O and O_2 diffusion efficiently, the molecular dimension of the barrier materials should be comparable to those of the H_2O while it also should be chemically stable in contacted with H_2O, O_2, acidic, neutral or alkaline solutions. Considering these requirements, the ALD novel BeO film in the nanometer thickness range was investigated as a potential gas diffusion and anti-corrosion barrier with nanometer thickness. The unique combination of properties and specific characteristics of BeO (see Table 1) make this material a promising candidate for a variety of



Bulk properties of BeO
■ Energy bandgap: 10.6eV
■ Covalent bonding
■ High metling point(°C): BeO(2507), Al_2O_3(2072)
■ Small bond length (cm^3/mol)
:BeO(8.28) compared to Al_2O_3(25.8)
■ **Well known gas diffusion barrier**
■ Dielectric constant: 6.8
■ High thermal conductivity (W/m•K)
:BeO(300) compared to Al_2O_3(35), Gold (318)
■ Precursor: dimethylberyllium, $Be(CH_3)_2$

Table 1. Bulk properties of BeO

applications [16, 41]. Some of these characteristics include: 1. Superior performance at extreme temperatures – the material of choice for components requiring anti-abrasion at high temperatures. 2. Light weight, high rigidity and excellent thermal management properties which equate to better and more rapid heat dissipation over other ceramic materials. 3. The thermal conductivity is ten times greater than that of the alumina ceramics, making it useful in heat producing circuits, such as those carrying high currents or of very high density. 4. A stable dielectric constant allows for improved electrical performance, particularly at higher frequencies. 5. BeO bulk ceramics are well known gas diffusion and anti-corrosion barrier due to dense structure and chemical stability, which is used as a coating material of inner wall in the various reaction chambers. Even though BeO has many unique properties, it has not found widespread utility, in part due to the perceived toxicity concerns of Be, which may cause lung cancer. However, ALD BeO is stable and possesses no safety issues. In this paper, an assessment of the gas diffusion and anti-corrosion performance comparison between Al_2O_3 and BeO coatings grown by ALD at 200^oC is reported.

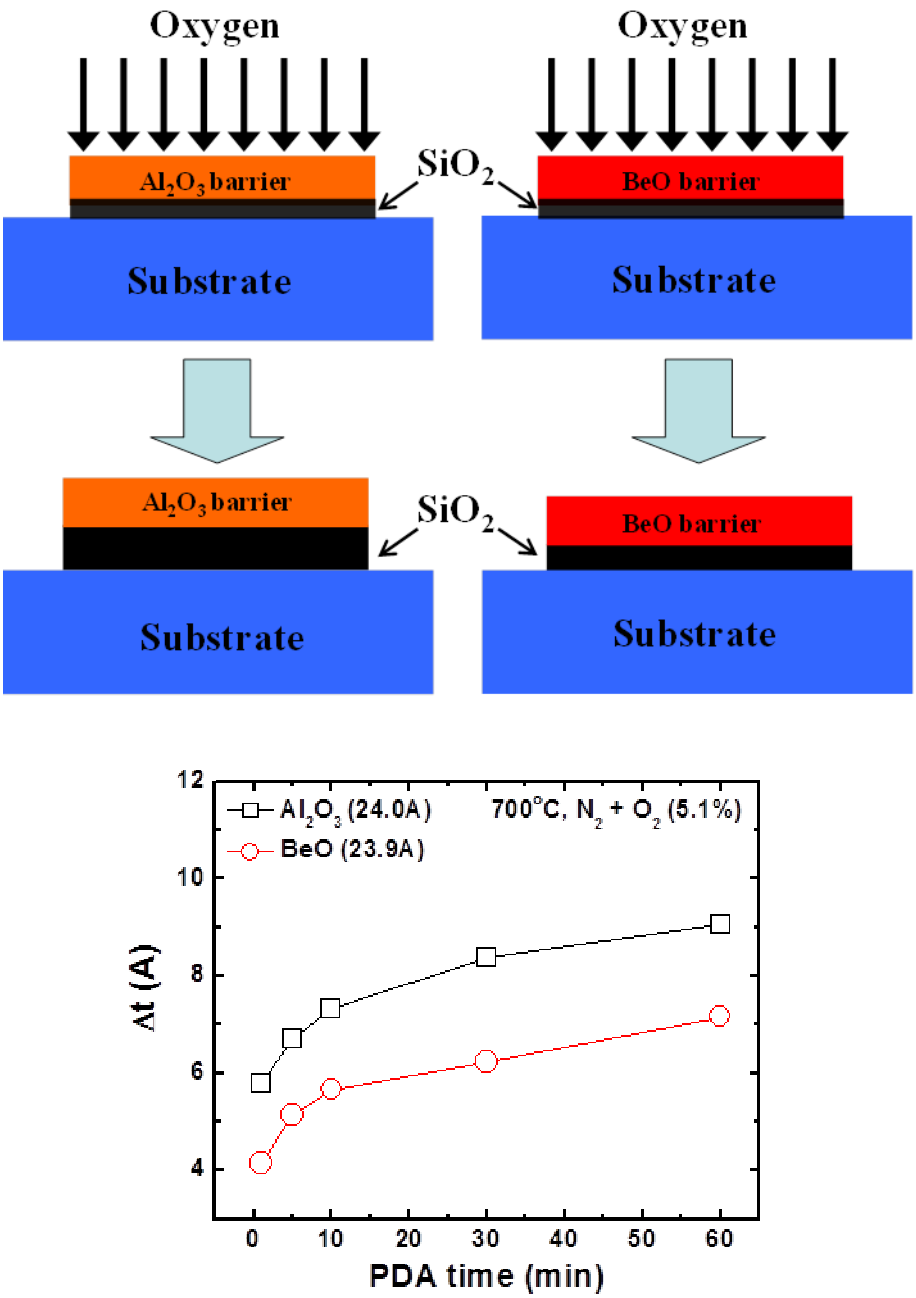


Fig 18. The schematic method and measured results to compare the oxygen diffusion rate between ALD Al_2O_3 and BeO. The native oxide (SiO_2) was growth at 700°C and N_2+O_2 (5.1%) ambient.

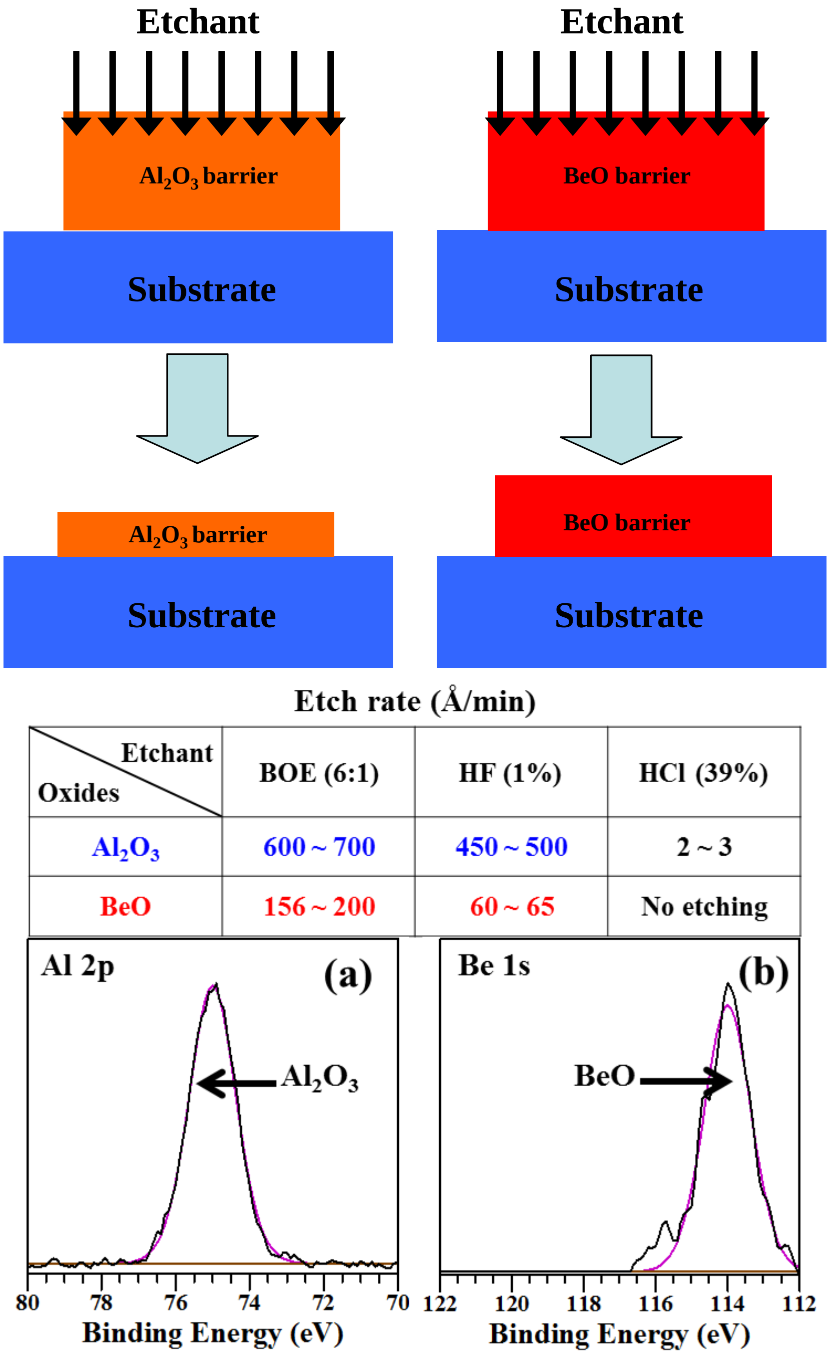
The BeO and Al_2O_3 ALD were performed in a hot-wall ALD flow reactor using sequential, self-limiting exposures to dimethylberyllium ($BeMe_2$) and trimethylaluminum (TMA) with water, respectively. A p-type Si substrate was cleaned with HF and SiO_2 (13.2 Å) was thermally grown, and loaded into the ALD reactor in a laminar flow hood operating at class 100 cleanroom conditions to minimize particle contamination. BeO and Al_2O_3 ALD growth temperatures were 200°C and the nitrogen gas was flown through the reactor at 20 sccm and produced a pressure of 0.2 Torr. A typical ALD cycle at 200 °C consisted of a 0.4 (0.025) sec $BeMe_2$ (TMA) exposure, a 5 sec purge, a 0.025 sec water exposure, and another 5 sec purge.

Due to lack of commercial tools for the oxygen transmission rates (OTRs) or water vapor transmission rates (WVTRs) measurements, we conducted the alternative experiments as schematically shown in Fig 18. By measuring the thickness of the SiO_2 layer after post deposition annealing (PDA) in N_2+O_2 (5.1%) ambient, the BeO and Al_2O_3 OTRs were compared. The data in Fig 18 shows that ALD BeO more efficiently prevents the oxygen diffusion as compared to ALD Al_2O_3. Thinner BeO under the same condition will show better throughput, compared to Al_2O_3. It is known that gas (including oxygen) diffusion through a thin film is proportional to the number of pinholes and pinhole size in the film. And, in general, materials with smaller molecular sizes have relatively smaller pinhole sizes [42]. The smaller pinholes cause more collisions between oxide and gas molecules during diffusion process, and result in the reduced permeation.

Both etch rate and permeation strongly depends on the molar density and binding energy of films. Therefore, evaluating anti-corrosion properties based on etch rates in several etchants is still valid to study the oxygen permeation characteristics. Fig 19 displays the measured etch rate and binding energy of ALD Al_2O_3 and BeO, respectively. Under the same amorphous phase, ALD BeO shows much lower etch rate, compared to

ALD Al_2O_3, which may be due to the higher binding energy of the valence electrons, responsible for the atomic cohesion of Al_2O_3 and BeO, that are Al 3p and Be 2s, respectively.

Oxygen diffusion is related to the molecular kinetics, and oxygen ion implantation also in the same principle. Therefore, it is valid to compare the oxygen ion implantation characteristics between BeO and Al_2O_3 films. Fig 20 shows the "SRIM" simulation results of oxygen ion (10 keV) implantation into BeO (10 nm)/Si or Al_2O_3 (10 nm)/Si stacks to compare the oxygen diffusion characteristics between BeO and Al_2O_3. SRIM is a group of programs which calculate the stopping and range of ions into target molecules using a quantum mechanical treatment of collisions [43]. This calculation is made very efficient by the use of statistical algorithms which allow the ion to make jumps between calculated collisions and then averaging the collision results over the intervening gap. During the collisions in Fig 20(a) and (b), the oxygen ions and BeO (or Al_2O_3) molecules have screened Coulomb collisions, including exchange and correlation interactions between the overlapping electron-shells. Comparing the penetration depth and damage profile between Al_2O_3 and BeO in Fig 20, the oxygen ions within the BeO target molecules have short range and narrow-spread interactions creating electron excitations and plasmons due to the high energy bandgap of BeO. These also can be described by including a description of the dense electronic structure of BeO.



Etch rate (Å/min)

Etchant / Oxides	BOE (6:1)	HF (1%)	HCl (39%)
Al_2O_3	600 ~ 700	450 ~ 500	2 ~ 3
BeO	156 ~ 200	60 ~ 65	No etching

Fig 19. The schematic and measured etch rate on BOE, HF, and HCl etchant, and binding energy comparison between ALD (a) Al_2O_3 and (b) BeO under the same amorphous phase, respectively.

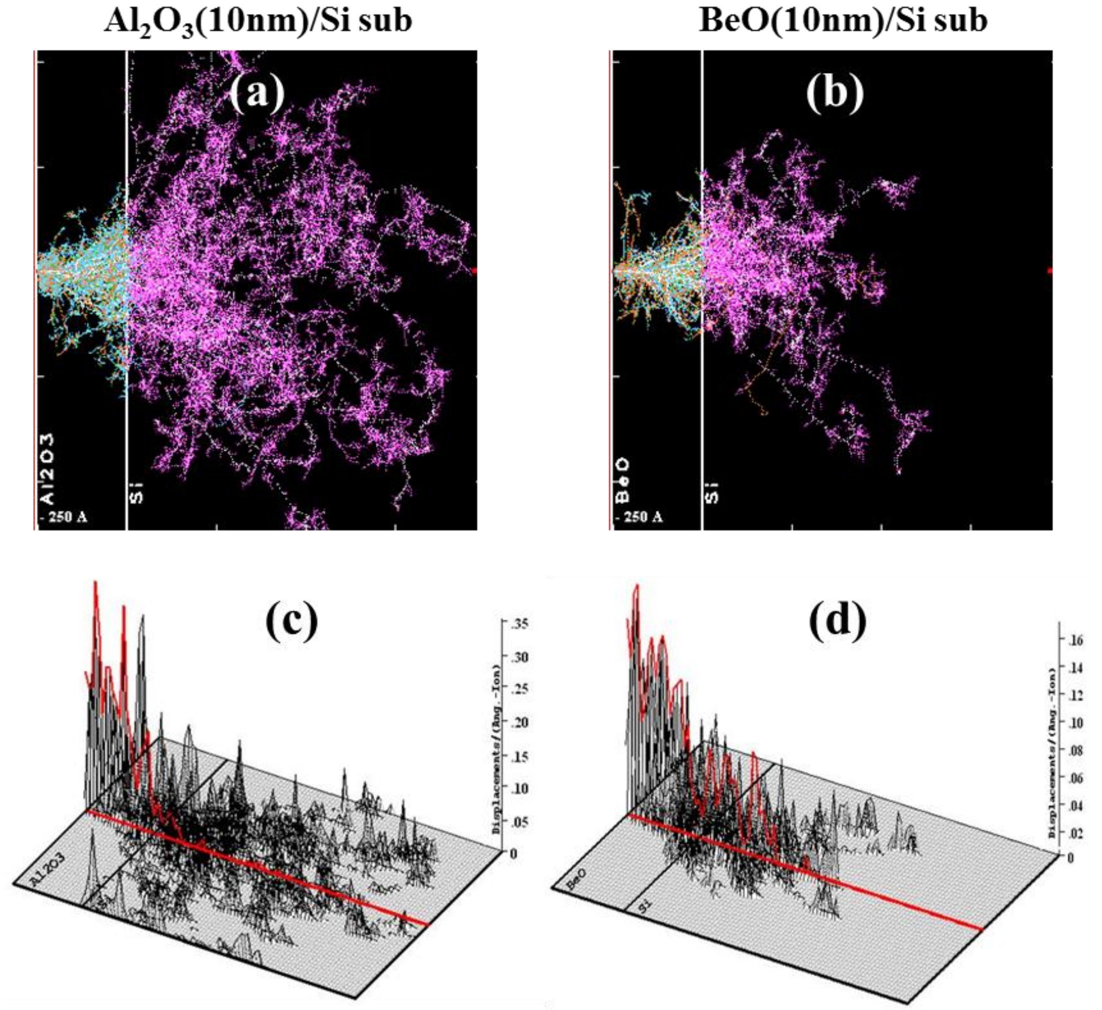


Fig 20. Oxygen implantation (10 keV) into (a, c)Al_2O_3/Si and (b, d) BeO/Si stacks to compare the oxygen diffusion characteristics. (a, b) plane and (c, d) 3D views of oxygen penetration depth and damage profiles.

In summary, ALD BeO was investigated as a potential gas diffusion and anti-corrosion barrier by measuring the growth rate of native oxide (SiO_2) and etching rates, respectively. And the quantum mechanical simulation was performed to compare the oxygen diffusion characteristics between BeO and Al_2O_3. These results support ALD

BeO is exceptional for the thin-film barrier layer and may find various applications as mechanical parts, packaging, and thin-film encapsulation technology for use in flexible organic electronics on polymers due to the small molecular size and high binding energy of BeO.

CHAPTER 4: Advanced Electrical Analysis of ALD BeO Gate Dielectric MOS Devices

4.1 BeO Interface Passivation Layer for Si channel MOS devices

To scale silicon based metal-oxide-semiconductor field effect transistors (MOSFETs), equivalent oxide thickness (EOTs) below 1nm are required for high performance technology nodes beyond 22 nm [1]. Therefore, the scaling of the interfacial passivation layer (IPL) between high-k dielectric and the Si channel plays an important role. As a possible solution, SiO_2 IPL thinning or scavenging can be induced during source/drain dopant activation annealing by introducing an oxygen absorption layer in an inter position within the gate stack [1, 2], and MBE grown SrO was studied as an IPL [3]. In this chapter, ALD BeO is used as an interface passivation layer (IPL) between channel and high-k gate dielectric. Fig 1 shows the fabrication procedures and schematic diagram of gate stacks with interface passivation layer (IPL).

- ■ **Diluted HF(1%) surface cleaning**
- ■ **ALD BeO(IPL) deposition at 250°C**
- ■ **ALD HfO_2 deposition at 250°C**
- ■ **RTA in N_2 between 500~600°C**
- ■ **PVD TaN deposition**
- ■ **Litho and dry etching**
- ■ **Backside contact**

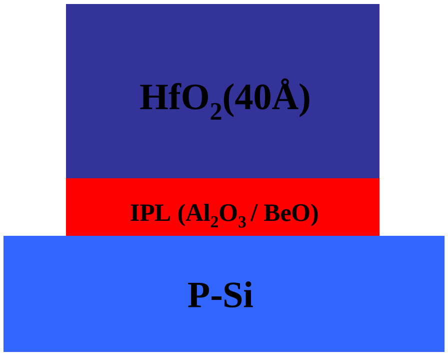


Fig 1. The fabrication procedure and schematic diagram of gate stacks with interface passivation layer.

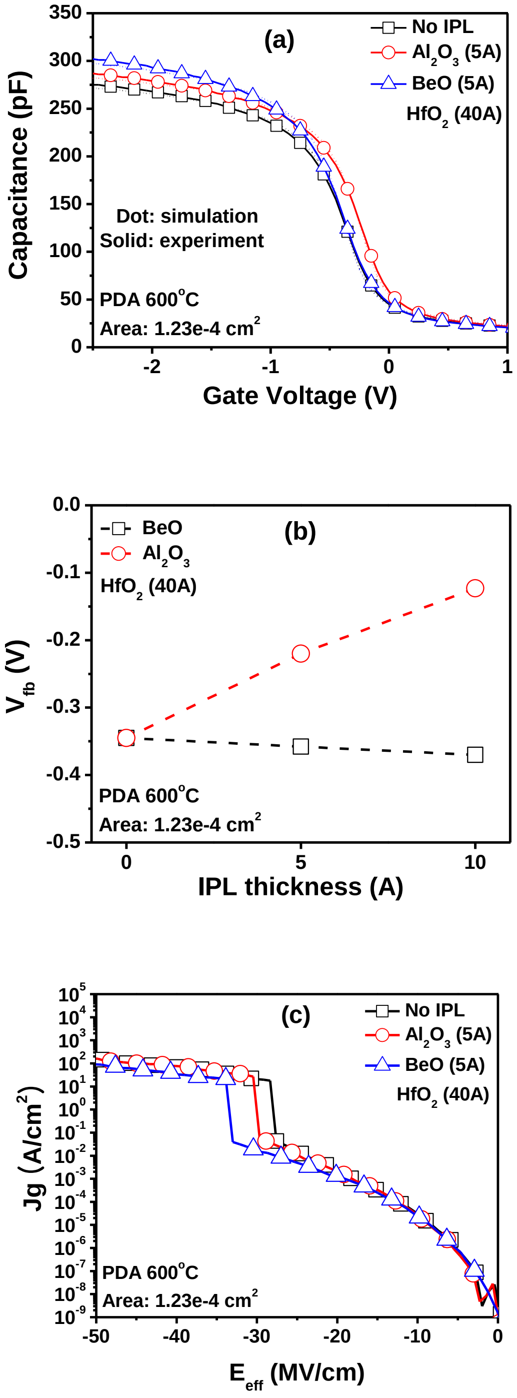


Fig 2. C-V and I-V characteristics of HfO_2, HfO_2/Al_2O_3 and HfO_2/BeO gate stacks on p-Si substrates.

Fig 2 displays the C-V and I-V characteristics of HfO_2(40Å), HfO_2(40 Å)/Al_2O_3(5 Å) and HfO_2(40 Å)/BeO(5 Å) gate stacks on p-Si substrates. In Fig 2(a), ALD BeO shows fair interface quality compared to the other gate stacks. In Fig 2(b), Al_2O_3 flat-band voltage (V_{fb}) increases as IPL thickness increases, but BeO is reverse. ALD Al_2O_3 is known that it has negative fixed charges [4]. Therefore, ALD BeO may have positive fixed charges. And BeO V_{fb} is less shifted with IPL increases, compared to Al_2O_3 cases. It may exhibit the lower amount of total fixed charges. In Fig 2(c), all gate stacks shows similar leakage current but ALD BeO shows higher breakdown field clearly compared to the other gate stacks. In Fig 3, BeO shows a smaller thermo-ionic current compared to that of the Al_2O_3. It may be due to the large energy bandgap of BeO.

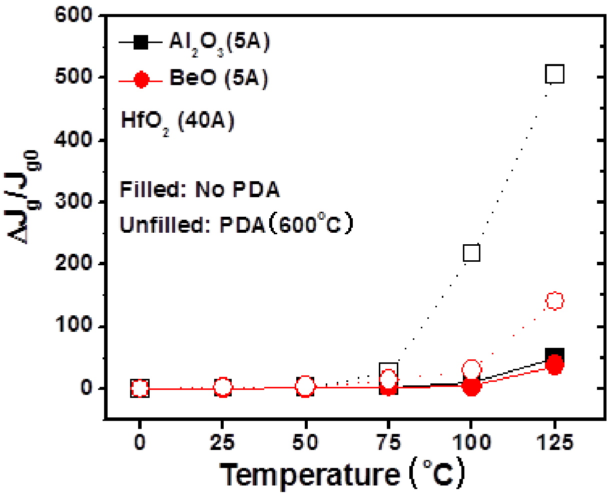


Fig 3. Thermo-ionic current comparison of HfO_2/Al_2O_3 and HfO_2/BeO gate stacks on p-Si substrates.

In Fig 4, PDA in N_2 atmosphere increases the EOT for HfO_2 and HfO_2/Al_2O_3 gate stacks due to the native oxide growth even PDA improves the dielectric constant of oxides. From Fig 4, HfO_2 and HfO_2/Al_2O_3(5Å) gate stacks show 3 ~ 4 Å and 2 Å SiO_x growth after 600 ^oC PDA, respectively. However, in contrast, HfO_2/BeO gate stack displays the EOT drop and both the lowest EOT and leakage current density after 600 ^oC PDA. After 900^oC PDA, HfO_2/BeO gate stack displays the EOT increase but still the lowest EOT compared to the other gate stacks. Thermally grown native oxide (SiO_x) on Si during PDA may be permissible for traditional CMOS technology. However, the PDA induced native oxides such as Ga_xO_y and As_xO_y on III-V substrates may have significant negative influence on the device performance [5]. *(For all practical purpose, EOT of BeO and Al_2O_3 samples are essentially the same with – 0.1nm difference)* Fig. 5 displays the schematic comparison of the IPL effect before and after PDA. The native oxide growth and oxygen vacancy generation in Fig 5 were based on the results in Fig 2 and 4. From Fig 5, ALD BeO effectively prevents the oxygen diffusion from HfO_2 and interfacial reaction during annealing up to 600 °C, while 0.5 nm thick Al_2O_3 film couldn't prevents oxygen diffusion, and consequently, increased the EOT.

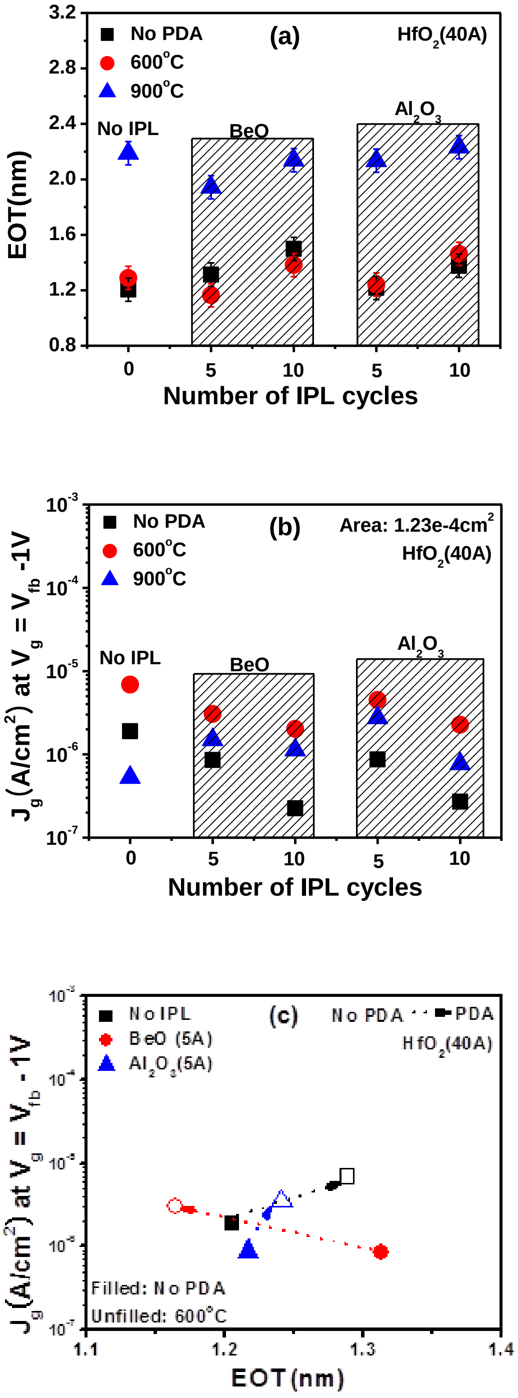


Fig 4. (a) EOT and (b) J_g vs the number of IPL cycles, and (c) J_g vs EOT between HfO_2, HfO_2/Al_2O_3 and HfO_2/BeO gate stacks with various PDA conditions.

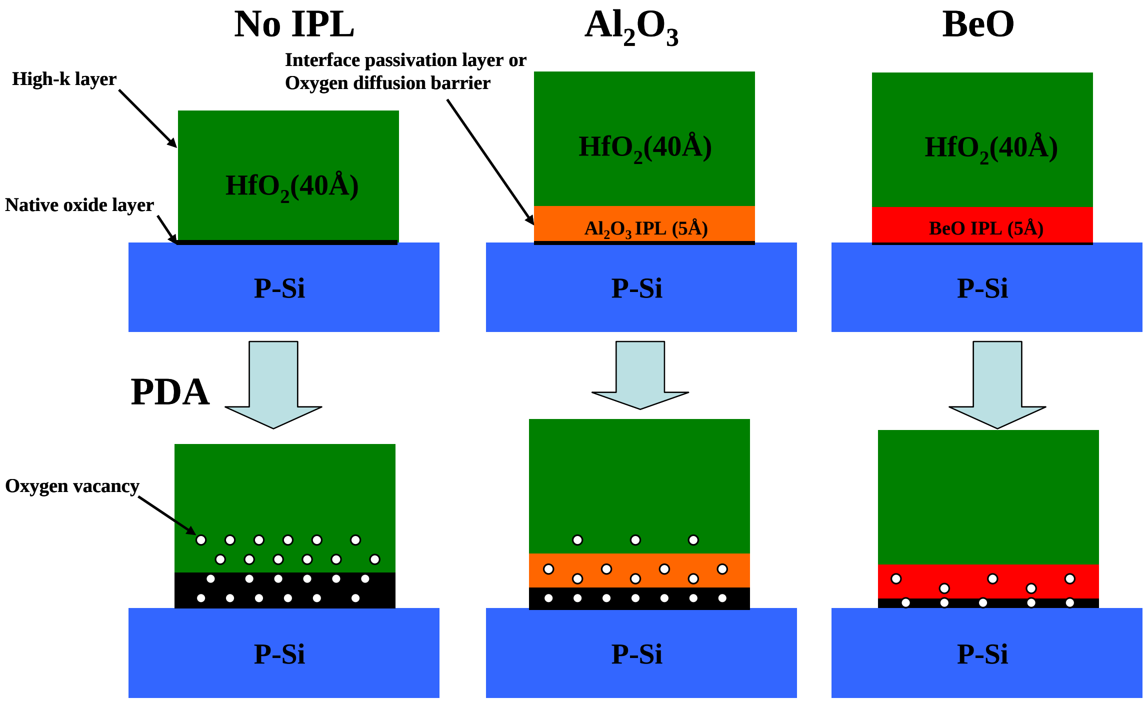


Fig 5. The schematic MOS structures to present the growth of interfacial native oxide and oxygen vacancy generation on HfO_2, HfO_2/Al_2O_3 and HfO_2/BeO gate stacks before and after PDA. The growth of interfacial layer and oxygen vacancy generation were estimated from results shown in Fig. 4 and XPS analysis.

It is generally known that oxygen vacancies within gate dielectrics are the origin of charge trapping and make worse the reliability characteristics [6, 7]. To investigate the interface quality on the three kinds of gate stacks in Fig 5, the typical methods, such as stress induced flat-band shift (ΔV_{fb}), stress induced leakage current (SILC) and time dependent dielectric breakdown (TDDB), were performed. Fig 6 displays ΔV_{fb} and SILC under the same effective stress field [$E_{eff} = (V_g - V_{fb})/EOT$]. For ALD BeO IPL in

Fig 6, it is more stable in terms of ΔV_{fb}, and also better immunity to FN stress was observed under the same E_{eff}.

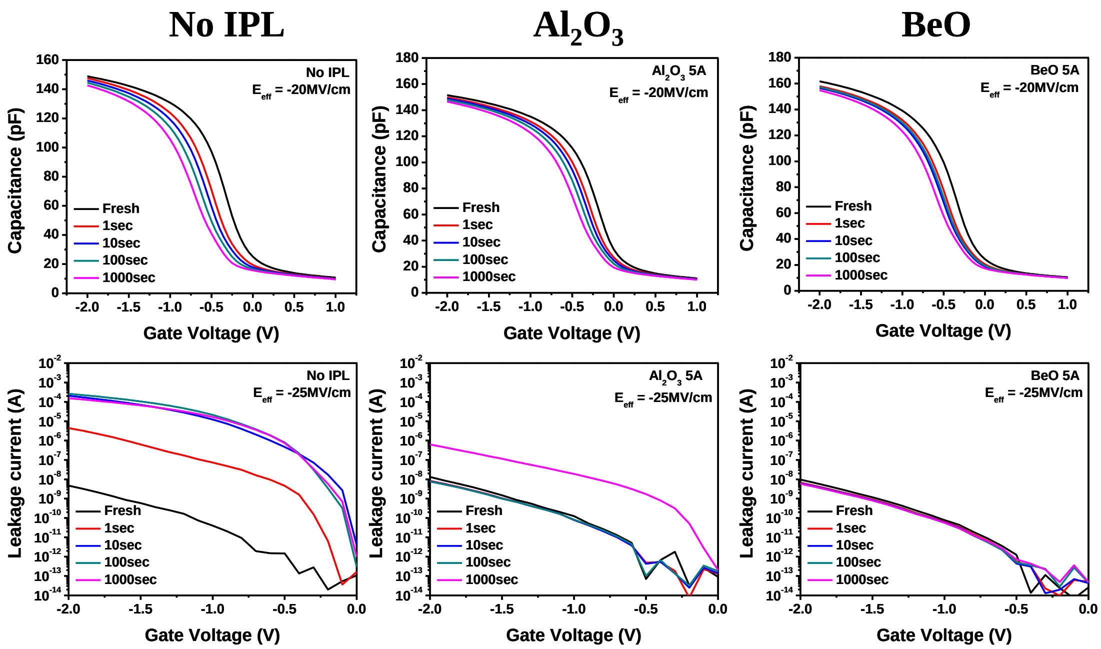


Fig 6. Stress induced Vfb shift (ΔV_{fb}) and stress induced leakage current (SILC) characteristics for HfO_2, HfO_2/Al_2O_3 and HfO_2/BeO gate stacks

Fig 7 shows the charge trapping characteristics of the three gate stacks. HfO_2, HfO_2/Al_2O_3 and HfO_2/BeO gate stacks display the start of breakdown at $E_{eff} = -21$, –24, and –26MV/cm, respectively. Unlike HfO_2/BeO gate stack, HfO_2 and HfO_2/Al_2O_3 gate stacks show the significant soft breakdown. Fig 8 is the summary and comparison of TDDB results for three gate stacks. The results in Fig 6, 7 and 8 suggest that ALD BeO may suppress the oxygen vacancy generation at the interface and gate dielectrics during PDA, and lead to the reliability improvement.

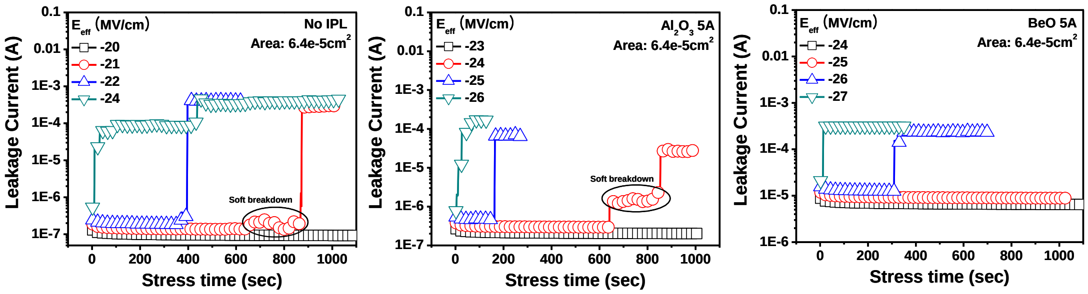


Fig 7. The time dependent charge trapping characteristics (TDDB) of the three gate stacks.

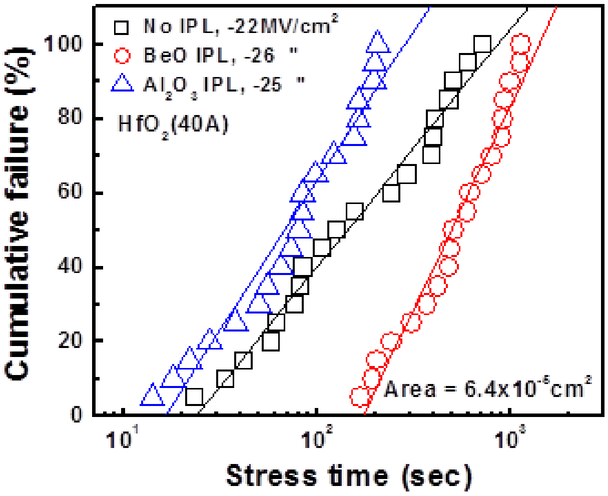


Fig 8. Time dependent dielectric breakdown (TDDB) comparison between three gate stacks.

4.2 Interface Passivation Layer for GaAs channel

Fig 9 shows the MOSCAPs fabrication procedures and schematic diagram of gate stacks with interface passivation layer (IPL) on p-GaAs substrates.

- **Diluted HF(1%) surface cleaning**
- **$(NH_4)_2S$ passivation**
- **ALD BeO(IPL) deposition at 250°C**
- **ALD ZrO_2 deposition at 250°C**
- **RTA in N_2 between 500 ~ 600°C**
- **PVD TaN deposition**
- **Litho and dry etching**
- **Backside contact**

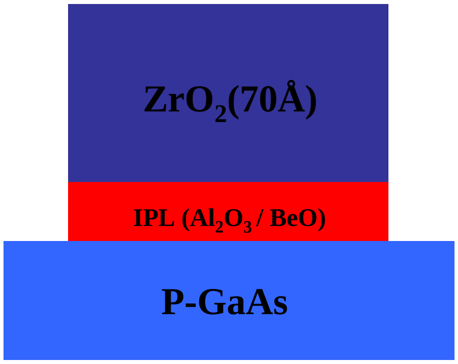


Fig 9. The fabrication procedure and schematic diagram of gate stacks with interface passivation layer.

Fig 10 displays the results of conductance measurements with the frequencies from 1MHz to 100Hz to compare D_{it} values between Al_2O_3 and BeO IPL. As shown in Fig 10, MOS devices with 5 (10) cycle BeO IPL have lower frequency dispersions of 42% (28%) on the accumulation region and smaller flat-band shifts of 0.5 V (0.4V) between 1MHz and 100Hz, compared with 66% (46%) and 0.7V (0.55V) in MOS devices with Al_2O_3 IPL. These comparisons indicate that there are fewer electronic defects at the BeO(IPL)/GaAs interface than at the Al_2O_3(IPL)/GaAs interface. The more self-cleaning reaction of ALD BeO precursor at the interface may reduce the native oxide of GaAs efficiently (shown in Fig 13 on chapter 3).

From the conductance measurement, D_{it} of 10 cycle BeO(IPL)/GaAs was estimated as $5.1\times10^{11}/cm^2eV$ at $V_g = V_{fb}+0.5(V)$, which is around two times lower than that of Al_2O_3(IPL)/GaAs ($9.03\times10^{11}/cm^2eV$) as shown from Ga 2p XPS in Fig 11. The condition of $V_g = V_{fb}+0.5(V)$ is selected due to the very high D_{it} at $V_g = V_{fb}(V)$. Full band analysis at the elevated temperatures and MOSFETs analysis will be presented in the future works.

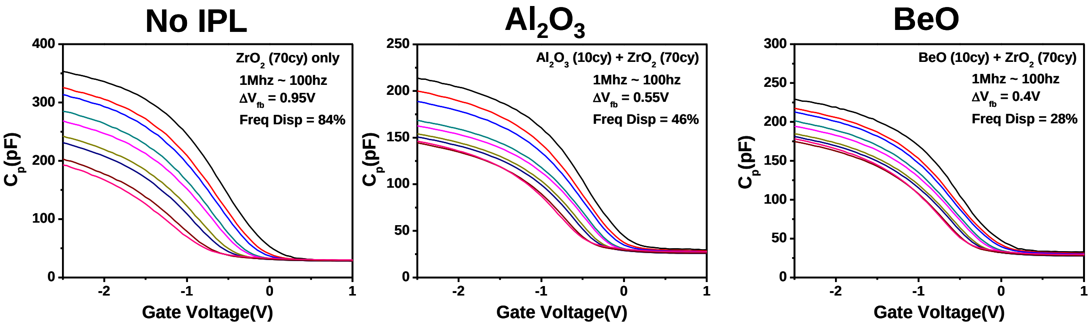


Fig 10. Conductance measurement for ZrO_2 with Al_2O_3 (BeO) IPL gate stacks for frequencies from 1MHz to 100Hz.

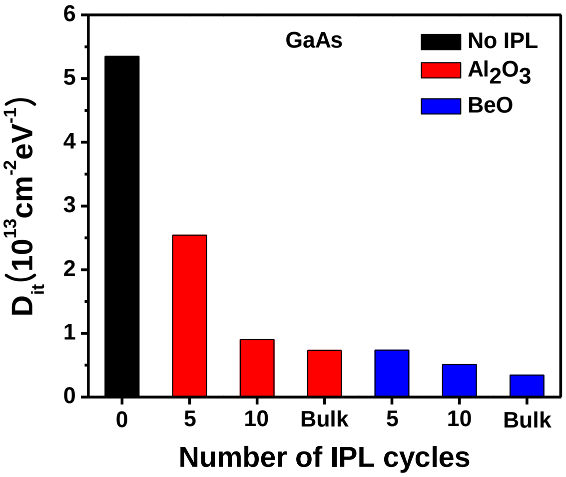


Fig 11. D_{it} extraction for ZrO_2 with Al_2O_3 (BeO) IPL gate stacks.

Figure 12 compares some electrical characteristics of BeO and Al_2O_3. Figure 12(a) shows the linear relation between the number of IPL cycles and the increase in the equivalent oxide thickness (EOT). The EOT may increase linearly with the number of IPL cycles because of the layer-by-layer growth mode of ALD BeO, unlike Al_2O_3 [8]. As shown in Fig. 12(b), the ALD BeO IPL has less hysteresis and frequency dispersion.

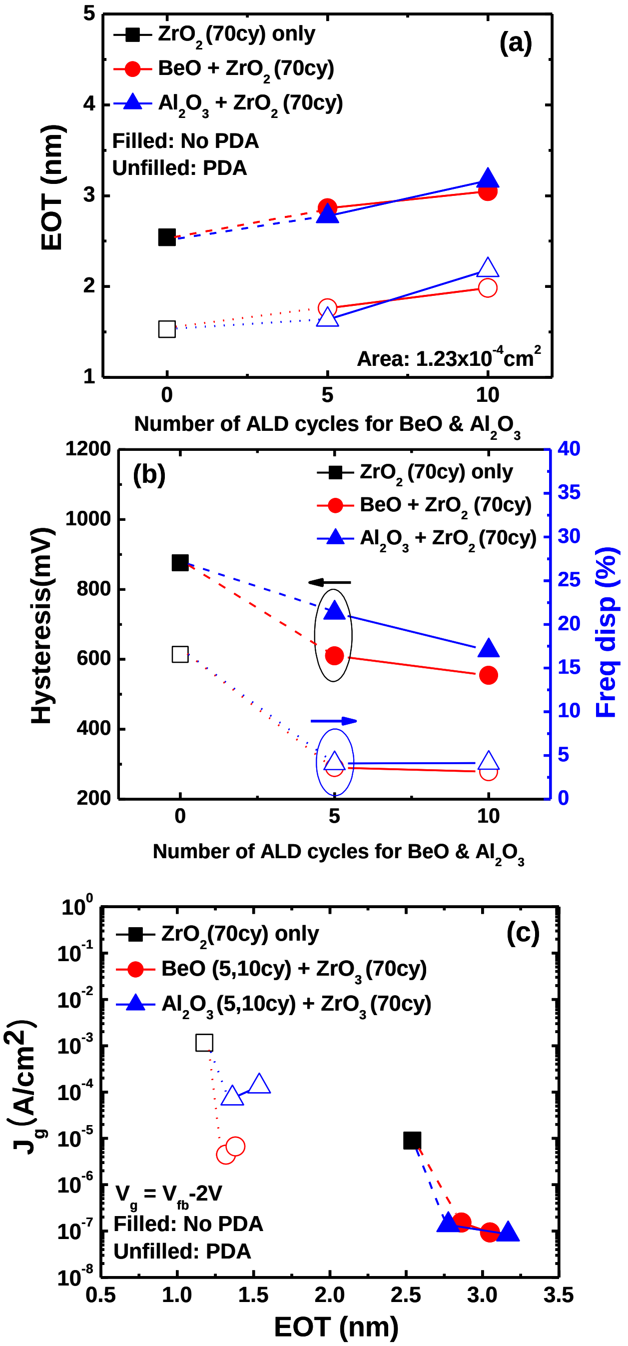


Fig 12. Comparison of (a) EOT, (b) hysteresis and frequency dispersion, and (c) J_g vs EOT of BeO and Al_2O_3 IPL using MOSCAPs.

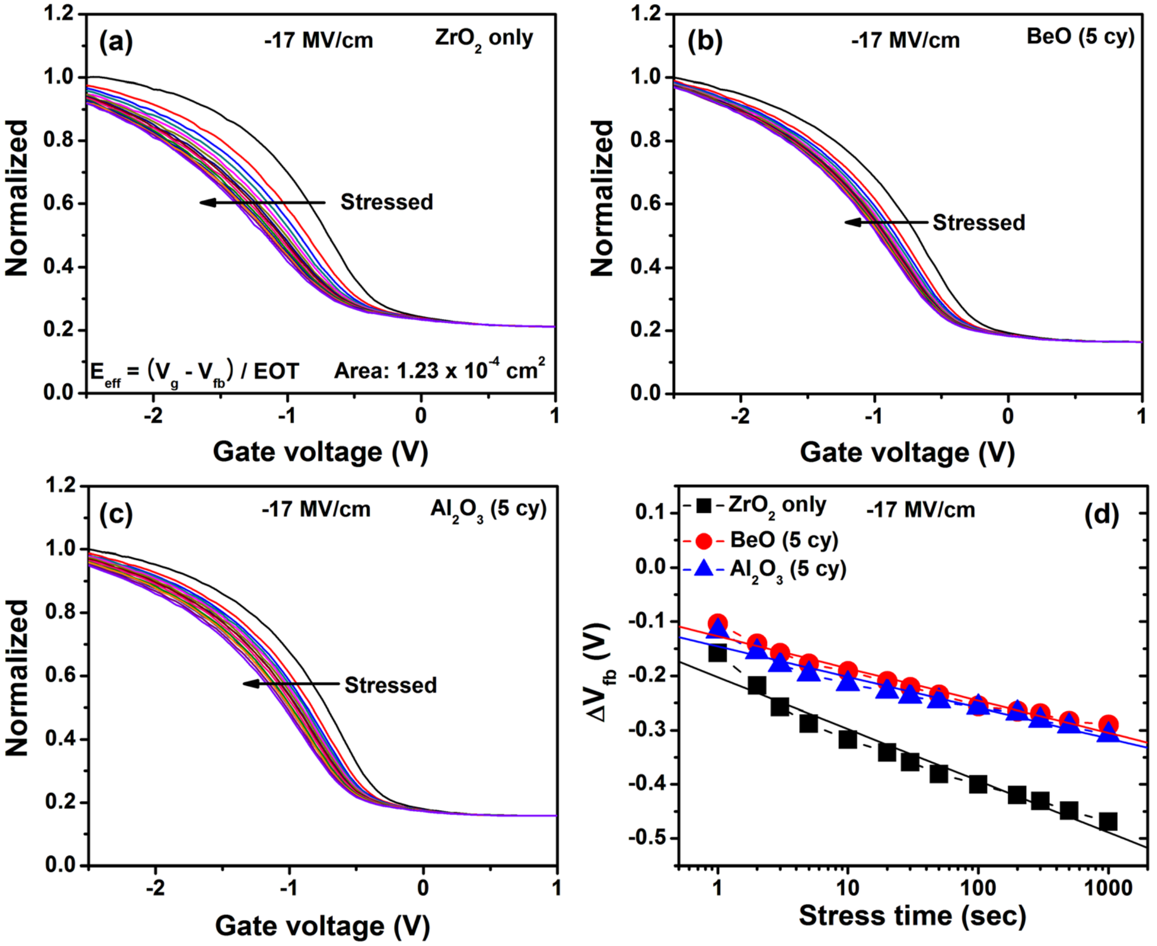


Fig 13. Comparison of V_{fb} shifts under the same effective stress field on (a) samples without IPL, (b) BeO, (c) Al_2O_3 IPL, and (d) a summary of three gate stacks.

The frequency dispersion was calculated using 1 MHz and 10 kHz CV characteristics; 10 kHz was selected due to the high frequency dispersion of 100 Hz. Figure 12(c) shows that suppression of the leakage current after PDA is more significant in an ALD BeO IPL, which is perhaps related to its higher thermal stability than Al_2O_3. Figure 13 shows the stress-induced flat-band voltage (V_{fb}) shift. Without an IPL (Fig. 13(a)), the V_{fb} shift is most significant, and both Al_2O_3 (Fig. 13(b)) and BeO IPLs (Fig. 13(c)) demonstrate improved V_{fb} shifts (Fig. 13(d)).

CHAPTER 5: Characterization of BeO Gate Dielectric Si MOSFET

5.1 Motivation of ALD BeO Interfacial Layer for Si MOS Devices

The CMOS scaling is bringing the SiO_2 thickness below 1.5nm. For these very thin oxides, the leakage current becomes unacceptably large. One way to reduce the leakage current is the substitution of the SiO_2 by a material with a higher dielectric constant. The main advantage of high-k dielectrics is the low gale leakage achieved due to its high physical thickness. That also makes it attractive for low power applications. Because of these requirements, over the past 10 years, hafnium oxide (HfO_2) has gained considerable interest as a high dielectric constant material for fabricating complementary metal oxide semiconductor (CMOS) devices. It has several attractive properties such as a high dielectric constant, good thermodynamic stability with Si, and good electrical properties [1]. Unfortunately, some of the other physical properties like mobility reduction, charge trapping and threshold voltage (V_{th}) instability are a major drawback for the performance of metal oxide semiconductor field effect transistors (MOSFETs) [2]. Especially HfO_2 high-k dielectric stacked MOSFETs were reported with low carrier mobility [3]. The main cause for the low mobility is still unknown, but has been attributed to remote Coulomb scattering caused by charges in the high-k dielectric [4] or optical phonon scattering [5]. Many researchers have believed that it is inevitable for all high-k dielectrics to have low energy bandgap and high scattering, compared to SiO_2. Therefore, if high-k dielectric with high energy bandgap and low scattering can be found, it will be the true solution for above problems.

An alternative promising high-k gate dielectric material is beryllium oxide (BeO), which has superior interface stability [6−10] and is already known as an excellent gas diffusion barrier. This makes it a potentially suitable diffusion barrier between HfO_2 and Si in CMOS processing. BeO also has metal-like thermal conductivity and a large energy bandgap (10.6 eV). These properties are indicative of low optical phonon and remote Coulomb scattering. Generally, a flow of phonons is responsible for heat conduction in dielectric materials. As the temperature increases, phonon density increases, but above 20 K, the phonon-phonon interaction becomes dominant and reduces the mean free path of the phonon drift, degrading thermal conductivity in the dielectrics [11]. BeO, however, has high thermal conductivity due to low phonon scattering because electrons in BeO are tightly and closely bound, so that the phonons in BeO are coupled to each other and have low energy and long wavelengths (or low phonon frequency). The high energy bandgap of BeO makes intrinsic charge trapping difficult and results in a low fixed charge in the BeO dielectric (fixed charges in high-k dielectrics are the source of Coulomb scattering) [10]. Our previous studies have showed electrical and physical characteristics that BeO deposited with dimethylberyllium and water improves interface quality on III-V MOS devices by preventing sub-oxidation between high-k and III-V substrate during PDA [6]. In this paper, we compare the effect of interfacial barrier layer by inserting ultrathin SiO_2, Al_2O_3 or BeO barrier layer (IL) between the HfO_2 gate dielectric and Si substrate in metal oxide semiconductor capacitors (MOSCAPs) and NMOSFETs. The aim of using such a barrier layer was to improve the device performance and reliability while maintaining, as much as possible, the overall dielectric constant of the resulting film.

5.2 Device Fabrication

An ALD BeO IL was deposited on HF-last p-type Si substrates using dimethylberyllium precursors and water as an oxygen source. As a reference, ALD Al_2O_3

IL was deposited on the same cleaned substrate using trimethylaluminum and the same oxygen source. Samples with a BeO IL, Al_2O_3 IL and without an IL were followed by ALD HfO_2. They were annealed for 3min at 600°C in N_2 at atmospheric pressure. The residual oxygen in the annealing furnace oxidized the metal layers. The physical thickness of the BeO and Al_2O_3 IL layers was controlled from the deposition rate which was measured on the bulk oxide using multiple-wavelength (200 ~ 900 nm) ellipsometry. The TaN electrode was deposited using reactive dc magnetron sputtering at 2000 Å followed by reactive ion etching (RIE) with Ar + CF_4 after electrode patterning of the gate. The source/drain (S/D) regions of NMOSFETs were implanted with phosphorus at 50 keV and a dose of $5x10^{15}$ cm^{-2}. High temperature (900 ^oC, 1 min) annealing in N_2 ambient was used for S/D activation. E-beam evaporated Ni/AuGe/Au was used for both S/D and backside metallization. The final sintering was done at 400 ^oC in forming gas for 30 min.

5.3 Results and Discussion

Fig. 1 shows the cross-sectional MOSFET structure and ring-type pattern. SiO_2, Al_2O_3, or BeO IL is placed between HfO_2 and the P-Si substrate. Al_2O_3 and BeO IL are intentionally inserted, but SiO_2 IL is thermally grown during post-deposition and S/D activation anneals.

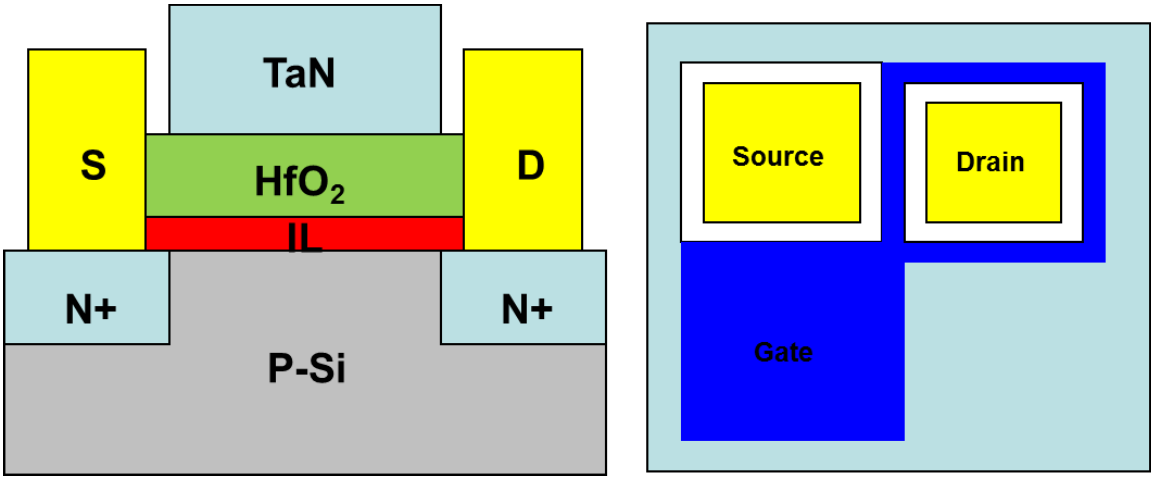


Fig 1. Cross sectional MOSFET structure and ring-type pattern. The BeO interfacial layer is placed between HfO_2 and p-type Si substrate.

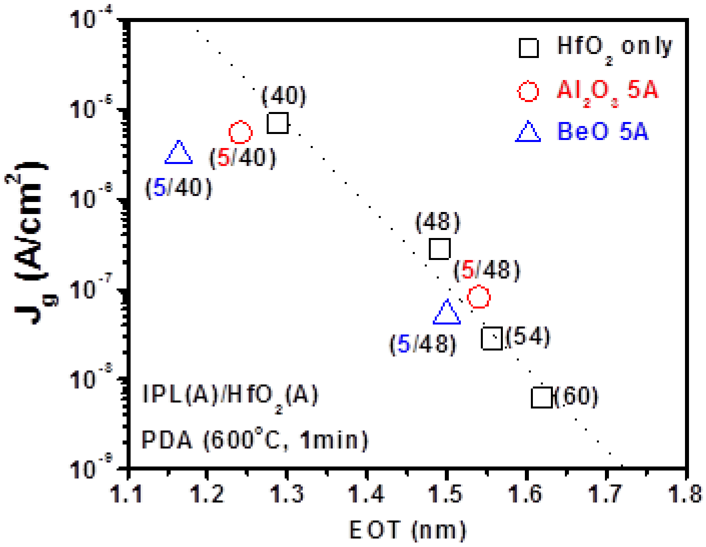


Fig 2. Gate leakage current vs EOT for SiO_2/HfO_2, Al_2O_3(IL)/HfO_2, and BeO(IL)/HfO_2 gate stacks.

In Fig 2, the BeO(IL)/HfO_2 structures show the lowest leakage, comparable to those of SiO_2(IL)/HfO_2 and Al_2O_3(IL)/HfO_2 gate stacks. Insertion of BeO IL (5 ~ 10 Å) doesn't increase the EOT significantly after the post-deposition anneal (PDA) due to the efficient suppression of the oxygen diffusion during PDA. The effectiveness of oxygen diffusion barrier for BeO IL is more presented as the annealing temperature increases in Fig 3. BeO IL may have some advantage for EOT scaling and reliability improvement After S/D activation, around 15 Å SiO_2 is grown at the interface between HfO_2 and the Si substrate. The low EOT of BeO IL is an indication of efficient oxygen diffusion barrier. The similar results were presented using X-ray photoelectron spectroscopy (XPS) [10]. Oxygen diffusion through thin films is proportional to the number and size of pinholes in the respective film [12].

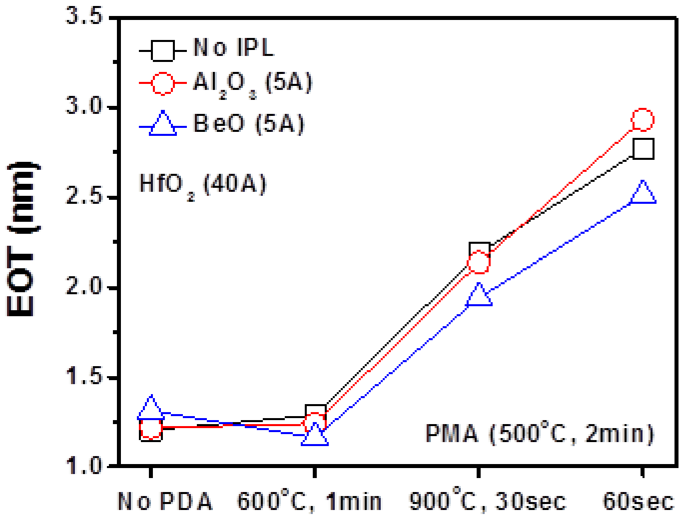


Fig 3. The change of EOT with the annealing temperature and duration for three different gate stacks.

In general, smaller pinholes cause more collisions between the diffusing molecules (e.g., oxygen) and the chemical groups present in the bulk film, reducing the rate of permeation. For reasons that are still under investigation, films of BeO, which have small molecular size, appear to exhibit relatively low oxygen diffusivity and are capable of effectively blocking the diffusion of impurities, such as Hf, thus minimizing defects in the substrate.

In general, the bandgap of the high-k material is inversely proportional to its permittivity, but BeO is an exception, having a very large energy bandgap (10.6eV) combined with a still high dielectric constant of 6.8. As the bandgap, or correspondingly, band offset increases, a charge trapping in the dielectric decreases. The effective potential barrier heights for SiO_2/HfO_2, Al_2O_3(IL)/HfO_2, and BeO(IL)/HfO_2 gate stacks are compared using the Fowler-Nordheim plot in Fig 4.

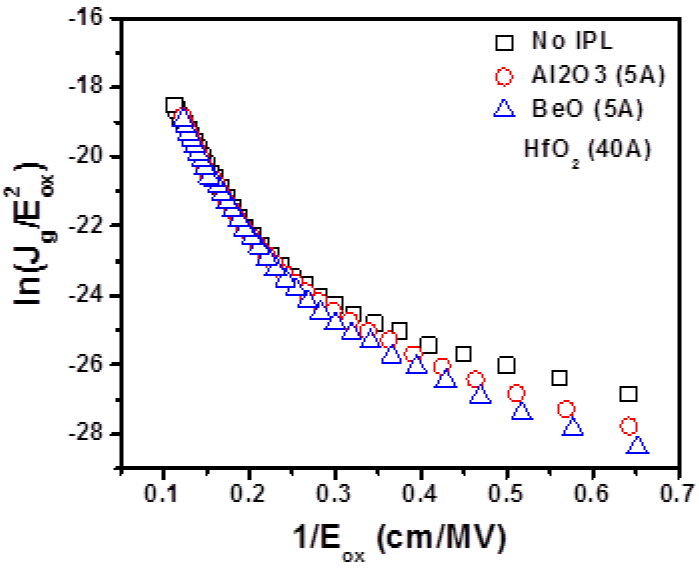


Fig 4. F-N plots to compare the effective potential barrier height for three different gate stacks.

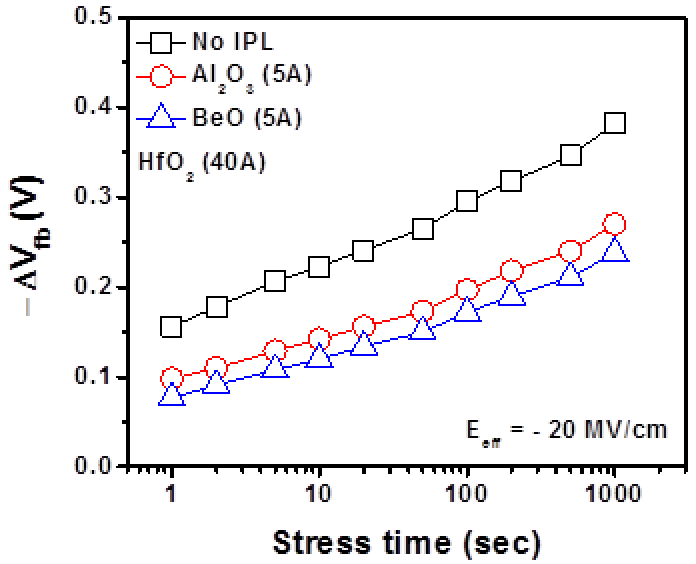


Fig 5. Stress induced V_{fb} shift (ΔV_{fb})vs stress time for three different gate stacks. $E_{eff} = (V_g - V_{fb})/EOT$

A higher barrier of the BeO IL stack is observed and it may results in the smaller electron tunneling currents, compared to other different gate stacks. In Fig 5, the BeO(IL)/HfO_2 gate stack shows less initial V_{fb} shift (after 1sec stress) indicating fewer pre-existing traps in the dielectric. A slightly smaller trap generation rate was also observed compared to other two gate stacks. In Fig 6, the BeO(IPL)/HfO_2 also shows the reduced stress induced leakage current (SILC) degradation and no soft and hard breakdown. But SiO_2/HfO_2 and Al_2O_3(IL)/HfO_2 shows gradual breakdown with stress time.

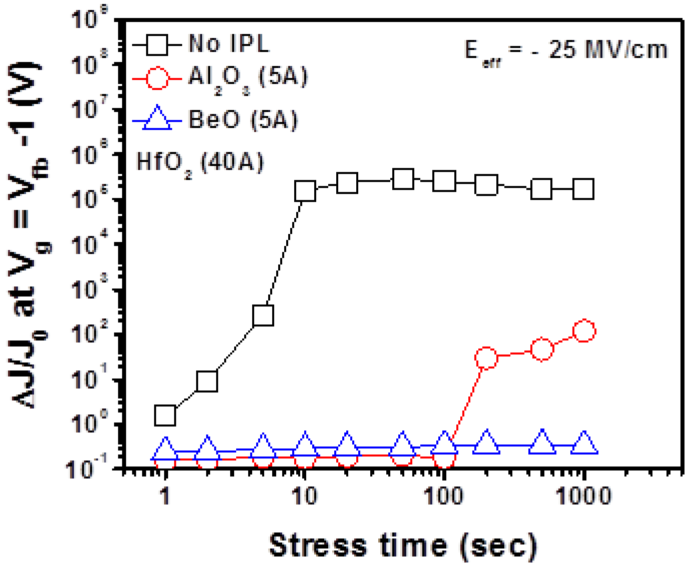


Fig 6. Stress induced leakage current ($\Delta J_g/J_0$) vs stress time. $E_{eff} = (V_g - V_{fb})/EOT$

The lower trap generation rate and the reduced tunneling current of the BeO(IPL)/HfO_2 gate stack may improve the reliability characteristics and it may be the indication of the high structural stability. In the view point of thermodynamics of materials, the total entropy of a material consists of its thermal entropy, which is related to thermal conductivity, and configurational entropy, which is related to the crystallization (or crystallinity) of the material [13]. With high crystallinity and thermal conductivity, BeO may have high total entropy, and it means that BeO is more structurally stable, compared to other gate dielectrics, even though the correlation between thermodynamic stability and device performance is still questionable.

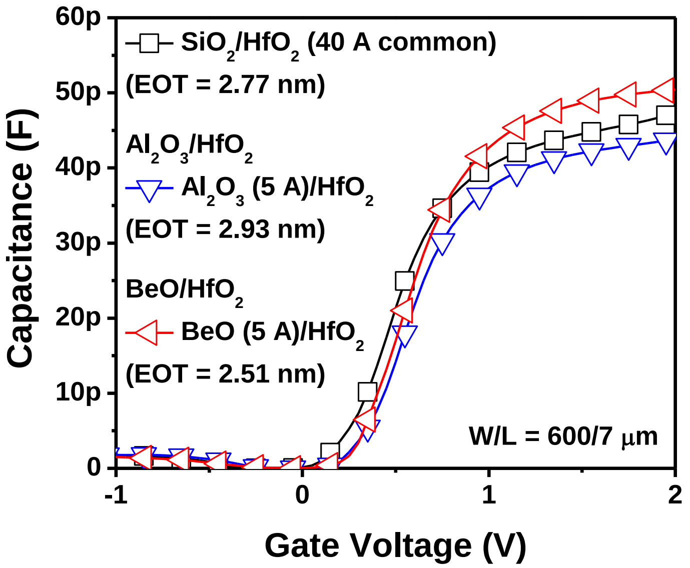


Fig 7. NMOSFETs inversion capacitance for three different gate stacks.

Fig. 7 is NMOSFET inversion capacitance for SiO_2/HfO_2 (40 Å), Al_2O_3(5 Å)/HfO_2 (40 Å) and BeO(5 Å)/HfO_2(40 Å) gate stacks. The BeO/HfO_2 gate stack shows a slightly lower equivalent oxide thickness (EOT) (2.51 nm) than SiO_2/HfO_2 (2.77 nm) and Al_2O_3/HfO_2 (2.93 nm) even though the EOTs for all gate stacks significantly increased after S/D activation annealing (Fig 3). From the XPS analysis, EOT increase is mainly due to the oxygen in HfO_2 dielectric, instead of oxygen residue in anneal tool [10]. Fig. 8 shows NMOSFET drain current- gate voltage (I_d-V_g) characteristics of SiO_2/HfO_2, Al_2O_3/HfO_2, and BeO/HfO_2 gate stacks. With the slightly lower EOT, the BeO/HfO_2 stack exhibits more positive V_{th} (0.66 V), higher drive current at V_g = 2 V, and better subthreshold swing (69 mV/dec), compared to those of the SiO_2/HfO_2 stack (V_{th} = 0.37 V, SS = 77 mV/dec) and Al_2O_3/HfO_2 stack (V_{th} = 0.46 V, SS = 70 mV/dec). The threshold voltage equation obtained from an ideal MOS structure [14] is

$$V_{th} = \Phi_{ms} - \frac{Q_i}{C_i} - \frac{Q_d}{C_i} + 2\phi_F$$

where Φ_{ms}, Q_i, Q_d, and ϕ_F are the work function differences between the metal and semiconductor (“–“ value), interface charge (“+” value), depletion charge (“–“ value) for the n-channel, and energy differences between the intrinsic energy level and Fermi energy level (+) for the n-channel, $Ø_F = (E_i - E_F)/q$. If we assume that Φ_{ms}, Q_d, and ϕ_F are the same for all gate stacks because the only difference is interfacial layer, then the positive shift of V_{th} of the BeO/HfO_2 stack is due to the less positive interface charges between BeO and the Si substrate. The fewer fixed charges in BeO layer may contribute to the fewer interface charges [10].

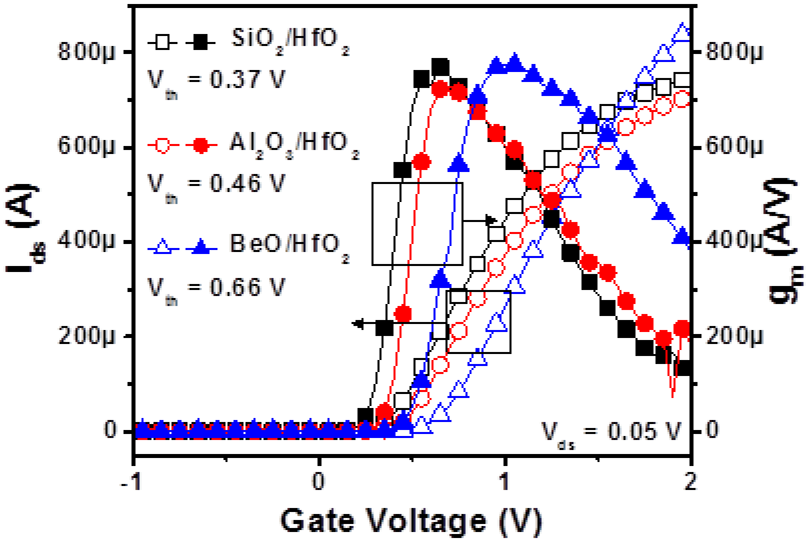


Fig 8. NMOSFETs I_d-V_g characteristics of three gate stacks. BeO IL shows slightly higher V_{th}, G_m, and I_d.

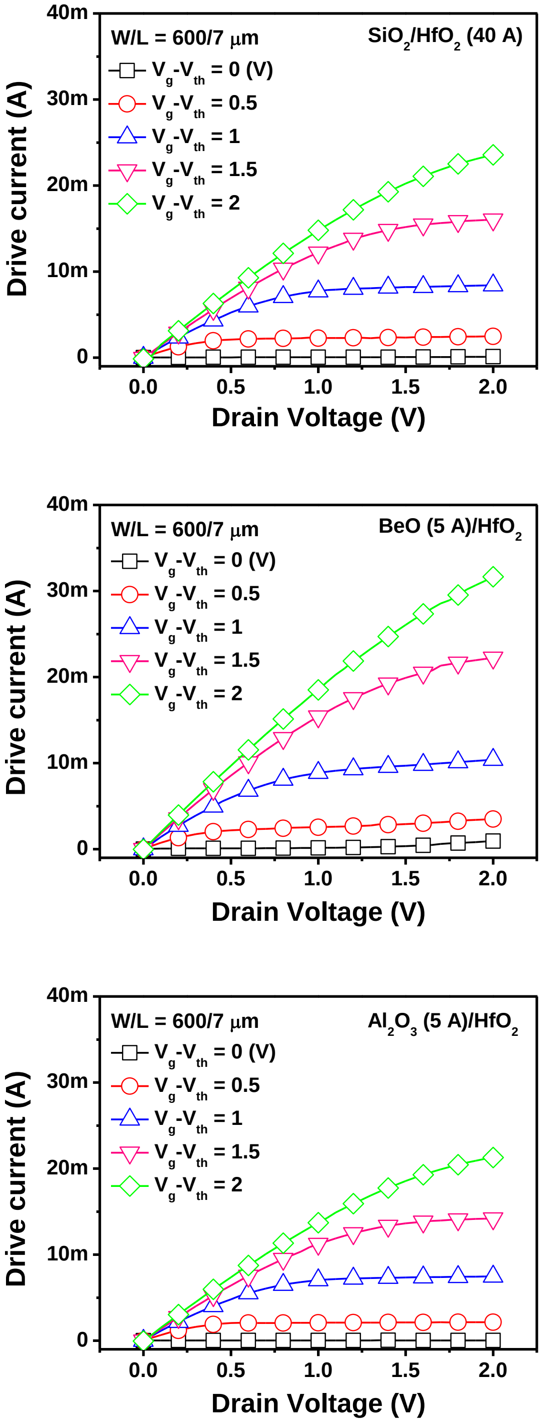


Fig 9. I_d-V_d characteristics of three gate stacks. BeO IL shows significant increased drive current compared to SiO_2 and Al_2O_3 IL gate stacks.

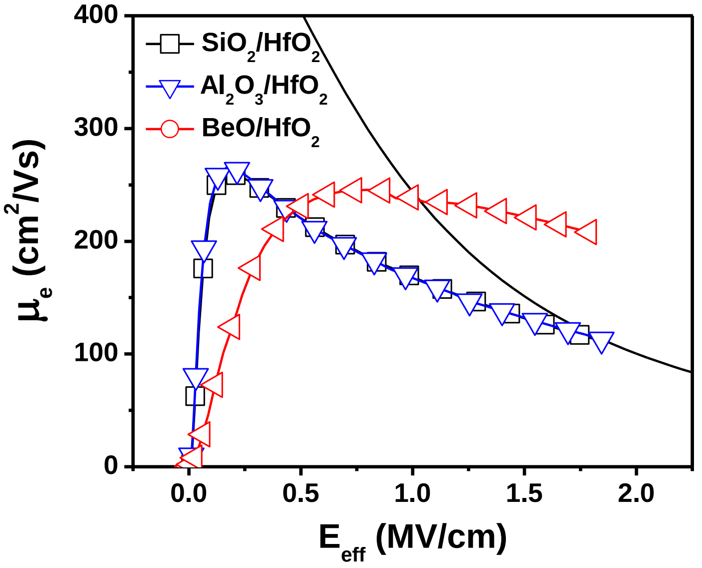


Fig 10. Effective channel mobility of NMOSFETs with three gate stacks.

In Fig 9, the BeO/HfO$_2$ stack shows around 34% higher drive current (31.67 mA) at V_d = 2 V & V_g–V_{th} = 2 V than the SiO$_2$/HfO$_2$ stack (23.56 mA) and Al$_2$O$_3$/HfO$_2$ stack (21.28 mA). There is some reduction of drive current with the IL thickness increase for both the Al$_2$O$_3$/HfO$_2$ and BeO/HfO$_2$ gate stacks, but it is more significant on Al$_2$O$_3$/HfO$_2$ stack. It may be due to the less native interfacial oxide (SiO$_2$) growth for Al$_2$O$_3$/HfO$_2$ stack. Fig. 10 illustrates the effective channel electron mobility using the split capacitance-voltage (C-V) method. The BeO/HfO$_2$ stack shows a 42% higher effective field (E_{eff}) mobility (238 cm^2/Vs) than SiO$_2$/HfO$_2$ (167 cm^2/Vs) and Al$_2$O$_3$/HfO$_2$ (166 cm^2/Vs) at E_{eff} = 1 MV/cm. The electron mobility in SiO$_2$/HfO$_2$ and Al$_2$O$_3$/HfO$_2$ are fast-saturated to the universal trend, likely due to the thick SiO$_2$ interfacial layer grown during S/D activation. If the SiO$_2$ interfacial layer is thinner, the peak electron mobilities of the HfO$_2$ gate stack will decrease significantly [15]. In a previous study, we demonstrated that ALD BeO on Si grows almost epitaxially [7], thereby improving electrostatic potential surface roughness, and may resulting in high field electron mobility.

In this work, a BeO (IL)/HfO_2 gate stack was investigated and systematically compared to a SiO_2/HfO_2 gate stack. Inserting an ALD BeO IL between the Si channel and high-k gate dielectric enhances high field carrier mobility and improves MOSFET parameter and reliability characteristics while maintaining a similar EOT. Excellent BeO properties, such as a high energy bandgap, efficient oxygen diffusion barrier, and high crystallinity, improve the charge trapping, the suppression in EOT increase during S/D activation, and MOSFET performance, thus imparting significant advantages to MOS devices with a BeO IL.

CHAPTER 6: Characterization of BeO Gate Dielectric InP MOSFET

6.1 Motivation for BeO gate dielectric InP MOS devices.

In this work, as an alternative of silicon substrate, Indium-phosphide (InP) has been studied. InP metal-oxide-semiconductor field-effect transistor (MOSFETs) have important potential applications in high-frequency digital circuits, microwave power amplifiers, and monolithic optoelectronics circuits. High electron mobility (5200 cm/V s) and high saturation velocity (2.5 × 107 cm/s) are the two key properties which make InP attractive for this application. The InP MOSFETs can be readily configured for enhancement-mode operation, thus allowing low-power dissipation to be achieved in digital circuits. As a result of the insulated gate, a large dynamic range for the circuit can be achieved leading to a larger logic swing and consequently better noise margins. The larger breakdown voltage, higher thermal conductivity, and lower ionization coefficient compared to GaAs make InP a better choice for microwave power generation. InP is expected to play an important role in optical fiber telecommunications since the long wavelength optical devices use InP as the substrate. Compared to GaAs, InP is far more suitable for MOSFET applications because the density of interface states near the conduction-band edge is small enough [1] provided that appropriate insulator formation condition is employed. A number of techniques have been used to fabricate these devices [2-6]. Early efforts also were directed at the development of an InP MOS technology using anodic [3-4] and thermal [5-6] oxides as gate insulators. However, the use of such oxides was abandoned due to the low resistivity ($r \approx 1012\ \Omega cm$) and large density of interface states near the mid energy gap (1-5~1011 cm-2 eV-1). To date, the best results for an InP MOS structure have been achieved with deposited dielectric layers such as:

SiO2 using direct and indirect chemical vapor deposition (CVD) [7-9], pyro-lyticy [10-11] and photo-CVD [12-13] techniques and with many efforts to passivate the surface in order to “unpin” surface Fermi level have been pursued [14-25].

Preliminary results show that ALD BeO grown on Si and GaAs is a promising candidate for interface passivation layer (IPL), displaying sufficiently high dielectric constant and lower interface defect density (due to the excellent self-cleaning effect) and leakage current density (due to the large conduction band offset), as well as excellent reliability and variability compared to Al_2O_3 IPL [26]. In addition, ALD BeO on Si substrate exhibits negligible hysteresis and frequency dispersion [10]. A focus of this study is investigating BeO gate dielectric on InP MOSCAPs and MOSFETs using ALD.

6.2 Device Fabrication

MOSCAPs were fabricated on n-type InP (100) with the doping concentrations of approximately $5 \times 10^{17}/cm^3$. After 1% HF dip surface cleaning, S passivation was performed by dipping in a 20% $(NH_4)_2S$ solution at room temperature for 10 min. Using this process, 50 ~ 120Å BeO was deposited as a gate dielectric at 250^oC using dimethylberyllium and H_2O as the precursors. As a reference, the similar thickness of Al_2O_3 was also deposited by ALD using trimethylaluminum and H_2O as the precursors. Then, post-deposition annealing (PDA) in the range of 500 to 550^oC was performed by a rapid thermal annealing (RTA) under N_2 ambient for 30 – 60 sec. In these devices, physical vapor deposited (PVD) TaN was used for gate electrode. After patterning and etching, post metallization annealing (PMA) was performed at 450^oC for 3 min in a forming gas ambient. Then, e-beam evaporated AuGe/Ni/Au alloy was used as the backside contact. The n-channel MOSFETs were fabricated on semi-insulating (SI) InP

(100) substrate with a ring-type pattern by gate last process (See Fig 1). The same surface treatment was performed on SI-InP as MOSCAPs, and then approximately 100Å Al_2O_3 as a dummy gate oxide was deposited by ALD 250°C. After 35 keV, $5 \times 10^{14}/cm^2$ Si ion implantation at the source and drain regions, samples were annealed at 730 ~ 770°C for 15sec for S/D activation. Then, Al_2O_3 layer was removed using buffered oxide etchant (BOE). After the same surface treatment on these InP samples, 90 cycles (110 ~ 120Å) ALD BeO was deposited as a gate dielectric. The TaN gate electrode was deposited by reactive sputtering of PVD. Finally, for source and drain metallization, around 600Å of AuGe/Ni/Au was deposited using e-beam evaporation.

6.3 Results and Discussion

Fig 2 (a) and (b) illustrates the typical C-V and I-V characteristics of InP MOSCAPs for Al_2O_3 and BeO samples. Similar physical thickness (around 80Å) was deposited both for Al_2O_3 and BeO, but after PDA, EOT was about 1 nm different between Al_2O_3 (EOT 4.4nm) and BeO (5.4nm) MOSCAPs. ALD Al_2O_3 shows the significant hump compared with BeO MOSCAP in the depletion region. Under the same effective electric field, ($E_{eff} = (V_g - V_{fb})/EOT$), ALD BeO displayed the lower leakage current density and higher breakdown field. Fig 2 (c) depicts the statistical analysis of TZDB for Al_2O_3 and BeO, respectively. In Fig 2(c), ALD Al_2O_3 exhibited a larger distribution of TZDB and a lower breakdown field than that for ALD BeO at 50% cumulative failure. But, at the upper values of cumulative failure, BeO and Al_2O_3 revealed similar breakdown fields.

(Gate-last process)

- 1% HF cleaning
- ALD Al_2O_3 (100A) capping layer deposition
- Align mark formation (photo-litho and etching)
- Photo-litho and ion implantation for S/D (n-channel) Si 40 KeV, $3x10^{14}cm^2$
- Removal of photo-resist and S/D activation using RTA (~750°C, 15sec)
- Removal of capping layer (BOE)
- Surface preparation (1% HF + $(NH_4)_2S$)
- Deposition of ALD BeO and PVD TaN
- Gate patterning (photo-litho and RIE)
- S/D contact formation (photo-litho and BOE)
- Metal deposition (AuGe/Ni/Au)
- Lift-off and annealing (450°C)

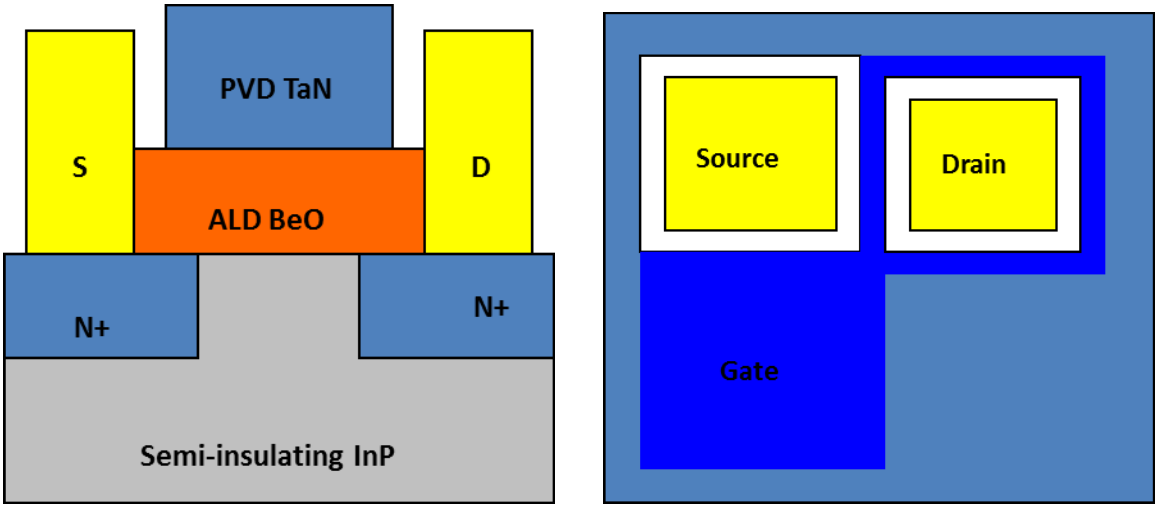


Fig 1. MOSFETs fabrication procedure and the schematic vertical and plane view of ring type transistor.

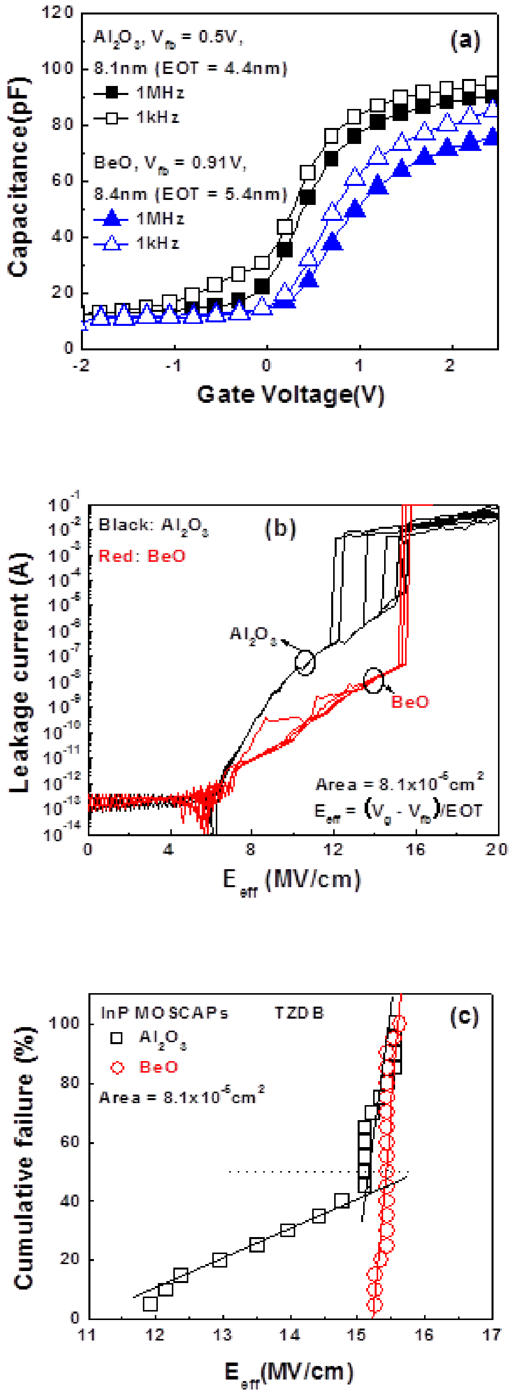


Fig 2. (a) C-V, (b) I-V and (c) Statistical TZDB characteristics of MOSCAPs on n-InP substrate using the gate dielectrics of ALD BeO and Al_2O_3 gate dielectrics, respectively.

Fig 3 shows the time dependent dielectric breakdown (TDDB) for Al_2O_3 and BeO MOSCAPs under the same effective stress field of 12.5MV/cm. The devices which show the early breakdown for Al_2O_3 and high initial leakage current for both Al_2O_3 and BeO were screened out. The life time of ALD BeO was approximately twice that of Al_2O_3 in the entire range of cumulative failure. And ALD BeO exhibited a soft breakdown (1st breakdown) unlike Al_2O_3, which only displayed a hard breakdown in Fig 3(b). Additionally, the average life time of the 1st breakdown for ALD BeO was close to that of the hard breakdown for ALD Al_2O_3. Fig 3(c) shows the characteristics of injected charges on devices at the 50% cumulative failure. The breakdown charge (Q_{BD}) for Al_2O_3 (3.7×10^{-5} C) was found to be three times larger than that for BeO (1.16×10^{-5} C), which may be related to the interface and bulk defect density. The efficient TZDB and TDDB of ALD BeO may be related to its atomic network or stoichiometry at the interface and in the bulk of the oxide.

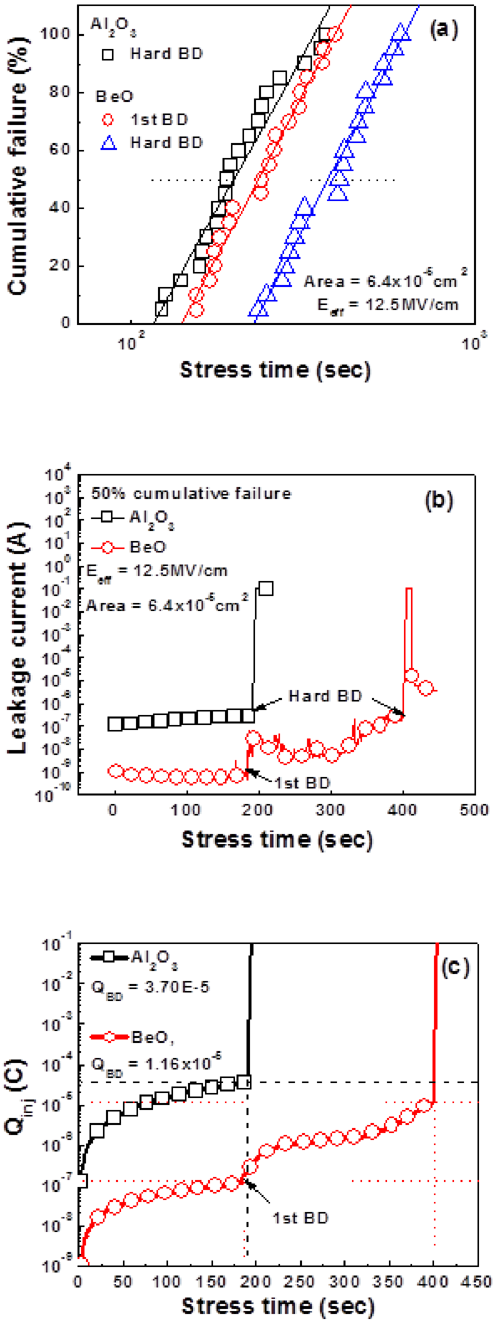


Fig 3. (a) Summary of statistical TDDB characteristics under the same effective stress field of 12.5MV/cm. (b) TDDB characteristics at 50% cumulative failure. (c) Calculated charge injection from TDDB results.

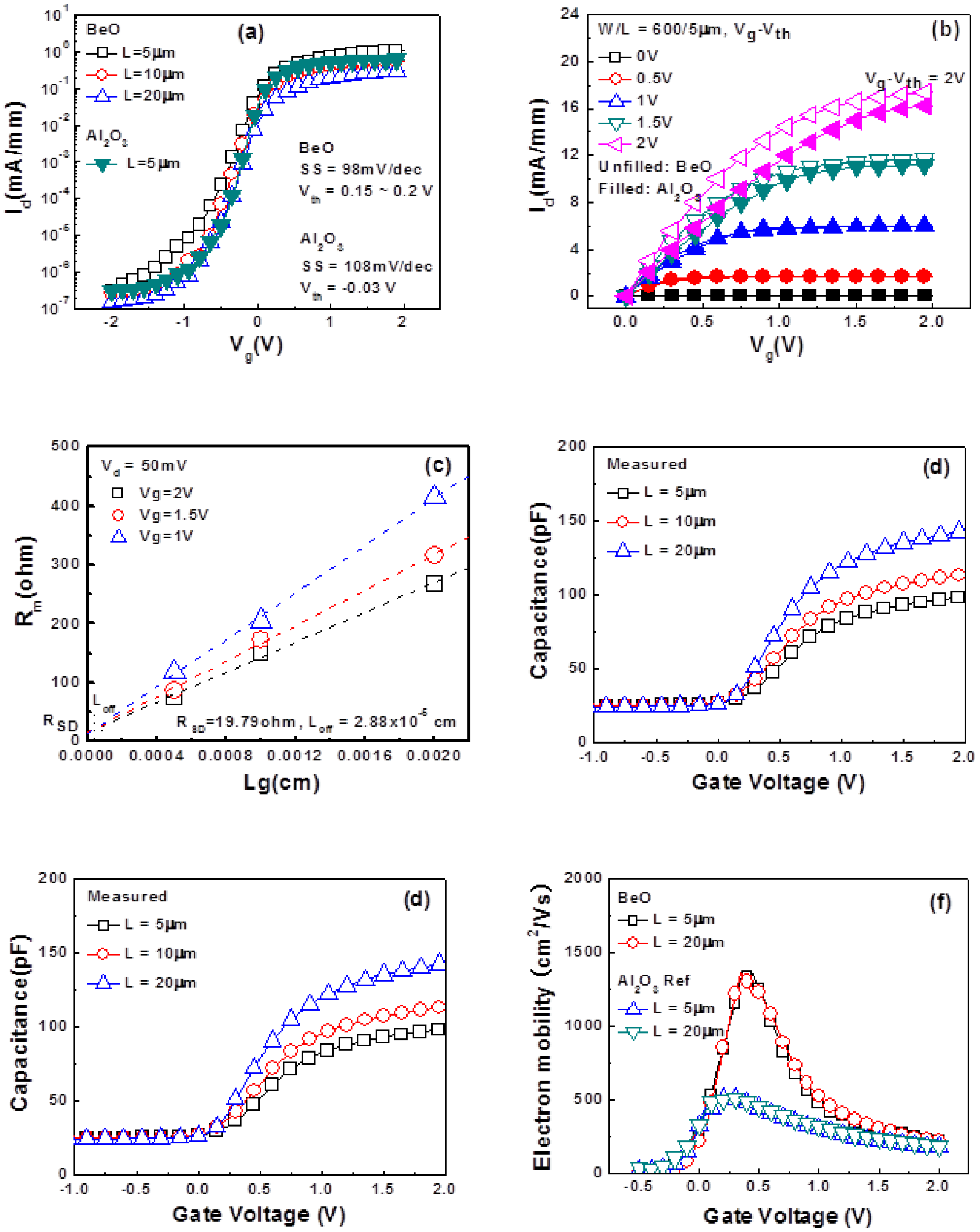


Fig 4. (a) I_d-V_g , (b) I_d-V_d, (c) Determination of length reduction and source/drain series resistance for BeO gate dielectric InP MOSFETs. (d) Measured split C-V, (e) Calculated split C-V after subtracting gate pad and S/D overlap capacitances, and (f) Effective electron mobilities as a function of gate voltage for various channel lengths.

Fig. 4 shows the characteristic of BeO gate dielectric on SI InP MOSFETs where the gate length (L) is 5, 10 and 20µm, and the gate width (W) is 600µm. Fig. 4(a) illustrate the I_d-V_g curve in a log scale. The V_{th} of BeO MOSFETs was between 0.15 and 0.2 V in the cases of L = 5, 10 and 20µm. But Al_2O_3 gate dielectric MOSFETs exhibited a slightly negative V_{th} (around –0.03 V, not shown). The minimum sub-threshold swing (SS) of BeO InP MOSFETs was 98 mV/dec for L = 10µm device, which was lower than the minimum SS for Al_2O_3 (108 mV/dec, not shown). The gate leakage current density of 8.56×10^{-8}A/cm^2 at V_g = 2V was obtained. Fig 4(b) shows the I_d-V_d characteristics as a function of gate bias. The gate voltage was varied from 0 to 2 V with a 0.05V step voltage. The off-drain current of 3.12×10^{-7}, 2.50×10^{-7} and 1.50×10^{-7} mA/mm, and current on/off ratio $[I_d(V_g = 2V)/ I_d(V_g = -2V)]$ 3.55×10^{6}, 2.21×10^{6} and 2.01×10^{6} were obtained for L=5, 10, 20 µm devices, respectively. Fig 4(c) shows the extractions of source/drain contact resistance (R_{SD} = 19.79Ω) and channel off-set (0.288µm), respectively. The overall resistance of a MOSFET in the linear region was plotted as a function of channel length, for various gate biases. This data revealed a well matched one point convergence of three linear fitted curves. Fig 4(d) displays the measured split CV of each device with 5, 10, 20µm channel length at the measuring frequency of 1MHz. The actual split CV in Fig 4(e) was calculated by subtracting the ring type pad capacitance and S/D overlap capacitance. The effective mobility in Fig 4(f) was calculated using a split CV (Fig 4(e)) and I_d-V_g curve (Fig 4(a)). The maximum effective electron mobility is approximately 1360 cm^2/V·s with EOT = 6.4nm. The measured electron mobility was 539 cm^2/V·s with EOT = 1.91nm (reference is 650 cm^2/V·s with EOT = 8nm [27] and 745 cm^2/V·s with EOT = 2.1nm [28]). The high interface quality of ALD BeO may improve the transport properties on BeO gate dielectric InP MOSFETs [26].

In this work, we presented our experimental results of ALD beryllium oxide gate dielectric based n-channel MOSFETs and MOSCAPs on InP substrates. The use of ALD BeO as a gate dielectric results in better interface quality contacted on InP substrates, as indicated by a thinner interfacial native oxide[10], positive threshold voltage, and improved the drive current, subthreshold swing and effective channel mobility. Ultimately, the use of ALD BeO as a gate dielectric or interface passivation layer may be an efficient solution for future III-V MOSFETs.

CHAPTER 7: Density Functional Theory Study of $Be(CH_3)_2$ Precursor

7.1 Motivation

The atomic layer deposition (ALD) of beryllium oxide (BeO) has been under investigation because BeO thin films have been proposed as interface passivation layers (IPLs) and high-k gate dielectric materials, in place of SiO_2 on Si and Al_2O_3 on III-V substrates [1-5]. In addition to its relatively high dielectric constant (k = 6.8) compared to SiO_2 (k = 3.9) and Al_2O_3 (k = 7.2), BeO also has a large band gap of 10.6 eV, which makes it an attractive gate dielectric [6]. Furthermore, BeO has other advantageous properties, including corrosion resistance [7].

In our previous study, ALD BeO, prepared using dimethylberyllium [$Be(CH_3)_2$] ($BeMe_2$) and water (H_2O), was found to display an efficient self-cleaning reaction at the interface between the BeO and III-V channel substrates. The study of the growth mechanism of ALD BeO is necessary to increase our understanding of the attendant surface chemistry and material properties.

7.2 Modeling for Surface Reaction and Discussion

In this study, we use density functional theory (DFT) to investigate an atomistic ALD mechanism along with the associated hydrolysis half-reactions on the BeO surface. Specifically, we used the Lee Yang Parr B3LYP [8] gradient-corrected function with the 6-31G polarization basis set for all atoms, which is generally used on ALD Al_2O_3 from TMA and H_2O [9]. All the calculations were performed using the Spartan 08 module [10], which automatically optimizes the molecular geometry.

The half-reactions between the precursors and the surface for ALD BeO formation can be expressed as follows:

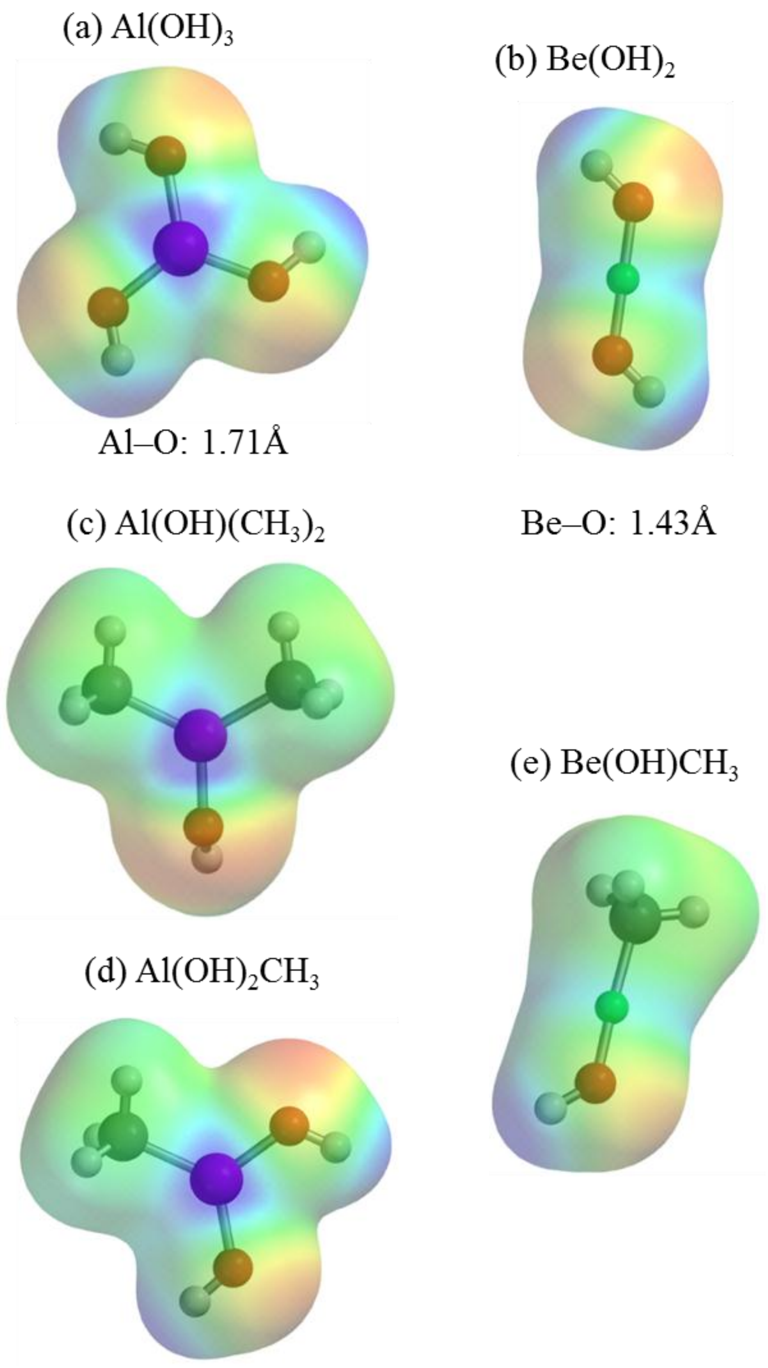
$$Be–OH^* + Be(CH_3)_2 \rightarrow Be–O–Be–CH_3^* + CH_4 \quad (1)$$

$$Be–CH_3^* + H_2O \rightarrow Be–OH^* + CH_4 \quad (2)$$

The asterisks denote the surface species. Above BeO reaction formulas are based on the well-known ALD Al_2O_3 reaction mechanism and the molecular structure of gas phase dimethylberyllium [11, 12]. In the literature, the reaction mechanisms of various cluster models are found to be the same [11]. Therefore, considering one reaction pathway is sufficient to establish what the ALD mechanism is [11]. Similar atomic properties between Be and Al tell that the utilized approach is sufficient to describe the surface reactions and capture all the relevant chemistry [13].

The two half-reactions occur in alternating cycles, with a purging period between them. We used $Be(OH)_2$ and $Be(OH)CH_3$ clusters to represent the Be–OH* and $Be–CH_3^*$ surface sites, respectively. These clusters enabled us to study the reaction energies at Be–OH* and $Be–CH_3^*$ sites, representing the electronic effects of the surrounding material of a model BeO surface. In addition, we also examined $Al(OH)_3$, $Al(OH)(CH_3)_2$, and $Al(OH)_2CH_3$ clusters to confirm the validation for the utilized models, and to compare the differences in potential surface energies as a reference. The results for reference here are in agreement with previous studies. All of the clusters are shown in Fig. 1. The reaction mechanisms involving BeO and Al_2O_3 are similar to those found using the $Be(OH)_2$, and $Be(OH)CH_3$ clusters. In particular, the gaseous precursors first molecularly adsorb by forming a complex, and CH_4 subsequently forms and desorbs. Moreover, the

$Be(OH)_2$ and $Be(OH)CH_3$ clusters adopt linear geometries as predicted for the divalent Be, in the gas phase, and occupy a smaller surface area, than trimethylaluminum (TMA)



(a) $Al(OH)_3$

Al–O: 1.71Å

(b) $Be(OH)_2$

Be–O: 1.43Å

(c) $Al(OH)(CH_3)_2$

(d) $Al(OH)_2CH_3$

(e) $Be(OH)CH_3$

Fig 1. Cluster models used in the calculations. (a) $Al(OH)_3$ and (b) $Be(OH)_2$ clusters representing Al–OH and Be–OH surface sites, respectively. (c) $Al(OH)(CH_3)_2$, (d) $Al(OH)_2CH_3$, and (e) $Be(OH)CH_3$ representing Al–CH_3 and Be–CH_3 surface sites, respectively

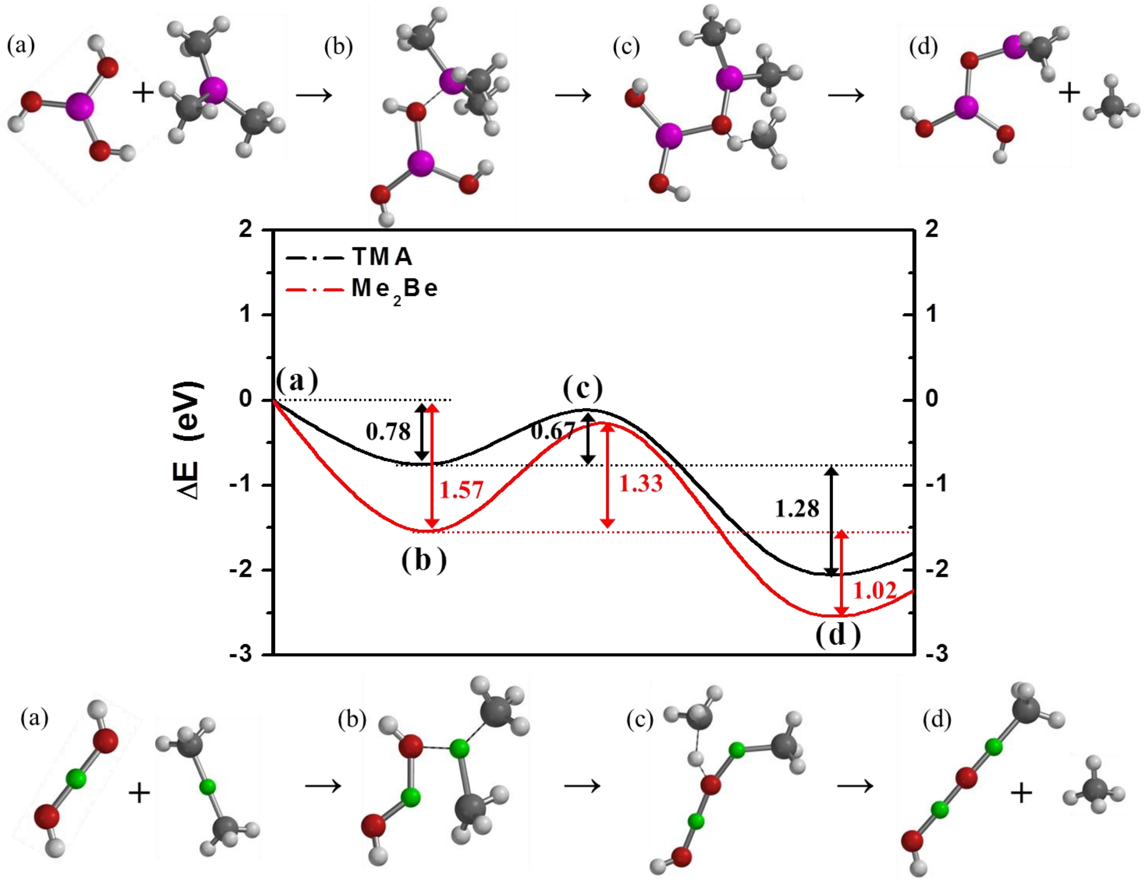


Fig 2. Reaction path and predicted energetics for reactions of $Al(CH_3)_3$ and $Be(CH_3)_2$ on the Al–OH* and Be–OH* surface sites. The stationary points correspond to (a) Al–OH + $Al(CH_3)_3$ and Be–OH + $Be(CH_3)_2$, (b) the $Al(CH_3)_3$ and $Be(CH_3)_2$ complexes, (c) the

CH_4 formation transition states, and (d) the Al–$(CH_3)_2$ + CH_4 and Be–CH_3 + CH_4 states, respectively.

clusters (see Fig 1). As a result, the former may afford a more ordered oxide layer after surface reaction. It is well matched with transmission electron microscopy (TEM) images

Reaction stages	$Al(OH)_3$ + $Al(CH_3)_3$	Reaction energetics (eV)	$Be(OH)_2$ + $Be(CH_3)_2$
(b) $Al(CH_3)_3$	-0.78	(b) $Be(CH_3)_2$	-0.96
(c) $Al(CH_3)_3$ + Al–OH	-0.11	(c) $Be(CH_3)_2$ + Be–OH	-0.24
(d) Al–$(CH_3)_2$ + CH_4	-2.06	(d) Be–CH_3 + CH_4	-2.59

Table I. Reaction energies for the Al–OH + $Al(CH_3)_3$ and Be–OH + $Be(CH_3)_2$ half-reactions, respectively. Energies are relative to the sum of the reactant energies.

of layer-by-layer grown BeO [2]. Reflecting the higher bond energy of the Be-O bond, distance was calculated to be 1.43 Å, which is less than the calculated Al-O bond distance (1.71 Å). High melting point, and short Be-O bond length in bulk BeO and gas phase $Be(OH)_2$ are the indication that Be-O may have a higher bond energy compared to Al_2O_3.

The potential energy surface (PES) of $Be(OH)_2$ + $Be(CH_3)_2$, representing reactions on Be–OH* surface sites, is shown in Fig. 2 with the corresponding energies listed in Table I. As can be seen in Fig. 2, $BeMe_2$ first adsorbs on a Be–OH* surface site, a process that is exothermic by 1.57 (0.78) eV. Compared to TMA, the adsorption of $BeMe_2$ onto the Be–OH* surface site may be easier. The molecular adsorption is an example of a Lewis acid-base interaction (Lewis adduct), with the Be centers acting as Lewis acids and hydroxyl residues (OH*) acting as Lewis bases [14]. Next, one methyl group from the adsorbed $BeMe_2$ reacts with one H atom from the surface –OH group to form CH_4, which subsequently desorbs. This step is preferable to chemisorbed $BeMe_2$ with an activation barrier of 1.33 eV and an exothermicity of 1.02 eV. The reaction of $Be(CH_3)_2$ on the Be–OH* surface has a higher activation barrier than TMA, which may be due to the relatively strong bond energy of Be-O, compared to Al-O.

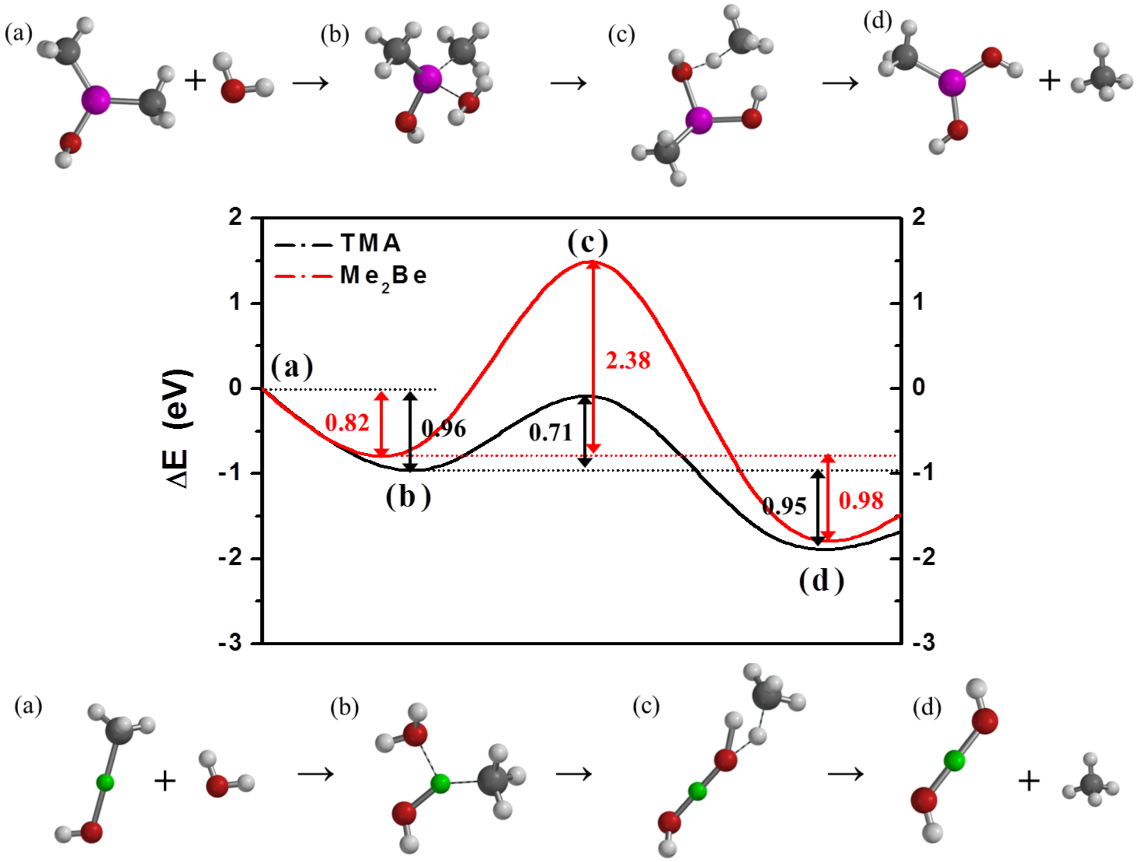


Fig 3. Reaction path and predicted energetics for reactions of H_2O on Al–$(CH_3)_2$ and Be–CH_3 surface sites, representing Al–CH_3* + H_2O and Be–CH_3* + H_2O half-reactions, respectively. The stationary points correspond to (a) Al–$(CH_3)_2$ + H_2O and Be–CH_3 +

H_2O, (b) the H_2O complexes, (c) the CH_4 formation transition states, and (d) the Al–CH_3 + CH_4 and Be–CH_3 + CH_4 states, respectively.

The reactions of $Be(CH_3)_2$ at the Be–OH* surface sites produce Be–CH_3 groups by replacing surface hydroxyl groups. We therefore investigated the reaction of H_2O with Be–CH_3* sites, which represents the second half-reaction, with the resulting PES shown in Fig. 3. The first pathway we investigated was the reaction of H_2O with a Be–(CH_3)* site. The reaction energies are shown in Table II. As can be seen in Fig. 3, H_2O first

Reaction stages	$Al(OH)(CH_3)_2$ + H_2O	Reaction energetics (eV)	$Be(OH)CH_3$ + H_2O
(b) H_2O complex	-0.96	(b) H_2O complex	-0.82
(c) Al–$(CH_3)_2$ + H_2O	-0.25	(c) Be–CH_3 + H_2O	1.56
(d) Al–OH + CH_4	-1.91	(d) Be–OH + CH_4	-1.80

Table II. Reaction energies for the Al–$(CH_3)_2$ + H_2O and Be–CH_3 + H_2O half-reactions, respectively. Energies are relative to the sum of the reactant energies.

adsorbs through the formation of a Lewis adduct at the Be–CH_3* surface site. This reaction was calculated to be exothermic by 0.82 (0.96 for TMA) eV. The H_2O adsorption is then followed by CH_4 formation and desorption, with a barrier of 2.38 (0.71) eV and a reaction energy of 0.95 (0.98) eV. Due to the high covalent characteristics of the Be-O bond, the resulting O-H bond in Be-O-H molecule may be stronger than that in H-O-H molecule, and thus result in the high activation barrier that was calculated. Similar reaction energy between Me_2Be and TMA may explain why $BeMe_2$ has an efficient self-cleaning reaction on the surface.

The adsorbed state for both half-reactions involves the formation of Lewis adducts between the precursors and the surface active sites. These adducts form between the oxygen lone-pair electrons and the empty *p* orbitals localized on the Be atom. Examination of the $Be(CH_3)_2$, and $Be(OH)CH_3$ structures indicate that these molecules exhibit linear geometries. This implies that one Be 2*s* and one Be 2*p* orbital hybridize to form two *sp* hybrid orbitals, which form bonds to the corresponding –OH and $–CH_3$ ligands, leaving two empty unhybridized 2*p* orbitals on the Be atom. These empty 2*p* orbitals then interact with the incoming H_2O lone pair in reactions between $Be–CH_3*$ and H_2O. The reactions between $BeMe_2$ and the Be–OH* surface site are similar except that the lone pair is located on the surface hydroxyl group, which interacts with the empty orbitals of the Be atom of the incoming $BeMe_2$ precursor. In the solid-state, $BeMe_2$ forms oligomers that exhibit 3-center-2-electron (3-c-2-e) bonds akin to both diborane (B_2H_6) and the TMA dimmer ($Al_2(CH_3)_6$) to satisfy the electron-deficient Be center. Similar to the complex formation observed in the ALD Al_2O_3, the energy of the complex in ALD BeO is higher than the final product energy. Equilibrium prefers the reaction products, rather than the intermediates, but the reaction is kinetically controlled due to the high energy barrier between the intermediates and the products. This means that the reaction is slow and long purge times are needed for the system to move toward the thermodynamically favored direction, unless elevated deposition temperatures are used.

7.3 Conclusion

In conclusion, we have proposed a detailed atomistic mechanism of ALD BeO using dimethylberyllium $Be(CH_3)_2$ and H_2O in the gas phase. We have presented the PES of both Be–OH* + $Be(CH_3)_2$ and $Be–CH_3*$ + H_2O with Al–OH* + $Al(CH_3)_3$ and Al–

CH_3* + H_2O half-reactions as a reference. We found that the Be related surface sites have higher activation barriers and reaction energies, possibly due to the increased covalent nature of the Be-O bond when compared to the Al-O bond. Furthermore, the reactions proceed through a stable intermediate complex before the formation and desorption of CH_4, resulting from the interaction between the oxygen lone-pair electrons and the empty *p* orbital of the Be atom.

CHAPTER 8: Summary and Future Work

8.1 Thesis Summary

My Ph.D. researches was devoted to three major studies. The first investigation was to understand the relation between interface quality and gate dielectric. From this study, several common requirements were found, such as thermal stability, energy bandgap, oxygen diffusion barrier, self-cleaning effect, low structural defect, low phonon scattering, and no “d” orbital. From a theoretical approach, BeO was found to be promising material as a gate dielectric due to low electromagnetic interaction between channel carriers and dielectric atoms, compared to other dielectrics. Growing high quality BeO film on Si and III-V substrates was a different challenge.

The second investigation was growing on high quality BeO film on substrates. To grow a thin film of BeO, several physical vapor deposition (PVD) methods including reactive sputtering and E-beam evaporation were attempted but all were unsuccessful due to high diffusivity of beryllium atom when their kinetic energy is high. Instead of the physical deposition, which has high kinetic energy, a chemical vapor deposition was employed in this study. However, due to the commercial unavailability of ALD BeO precursor, the desired BeO precursor ($Be(CH_3)_2$) was synthesized from $BeCl_2$ via Grignard metathesis, and subsequently utilized for the first time as an ALD precursor.

The last investigation was a material characterization and MOS device fabrication. The fundamental properties of ALD BeO film such as dielectric constant, energy bandgap and band offset, crystallinity and crystal structure, interfacial layer, oxygen diffusion barrier, and self-cleaning effect were studied. BeO gate dielectric MOS devices on Si, GaAs and InP substrates were studied and compared with Al_2O_3 gate dielectric MOS devices.

8.2 Suggestions for Future Work

In this PhD dissertation, only $Be(CH_3)_2$ was used as a BeO precursor. But this precursor is a solid and has some issues about the purity and ALD process controllability. Its initial purity is not high enough, and during the sublimation of ($Be(CH_3)_2$), there are some solid particles, at the beginning of the precursor use. Therefore, lots of pre-running is required to improve the precursor quality and to remove the remaining solid particles. However, $Be(C_2H_5)_2$ is a liquid, and it is more controllable as an ALD precursor. The purification process using distillation is easier due to its liquid phase. Therefore, it is strongly recommended to try ALD BeO based on $Be(C_2H_5)_2$ precursor.

The work can be extended to other application such as magnetic tunneling junction (MTJ) memory, thermal dissipation layer, SOI, TANOS, and ReRAM. BeO shows high crystallinity and good lattice match with Si substrate, so it is good candidate for MTJ and SOI application. And BeO has high thermal conductivity like metals. So it is a good candidate for thermal dissipation layer. The high energy bandgap of BeO is also useful as a barrier layer for TANOS and ReRAM applications.

APPENDIX: Theoretical Approach to Evaluating BeO as a Gate Dielectric

1.1 Thermodynamics Approach to Evaluating BeO

Based on the thermodynamic theory of materials, the total entropy, S_{total}, of a system consists of its thermal entropy, S_{th}, which arises from various ways in which the energy of the system can be shared among molecules, and its configurational entropy, S_{conf}, which arises from the number of distinguishable ways in which the molecules can fill the space available to them [1]. Thus

$$S_{total} = S_{th} + S_{conf}$$

Every material tends to minimize the internal energy. From thermodynamics, it is defined that the crystalline phase has lower internal energy than the amorphous phase. But there is an activation barrier between amorphous and crystalline phases, so as-grown ALD oxides are usually amorphous. Unlike other high-k dielectrics, as-grown ALD BeO exhibited high crystallinity on Si and GaAs substrates [2]. Consequently, BeO has low activation energy for crystallization which is related to its atomic or molecular configuration. Thermal entropy is proportional to the thermal conductivity. High thermal conductivity is the indication of high thermal entropy. In table II, BeO has the highest thermal conductivity, which is related to the high S_{th}. Therefore, the total entropy of BeO may be greater than the other dielectrics. The higher the entropy, the higher thermal stability is. In general, higher thermal stability is preferred, even though the correlation between thermal stability and interface quality is still uncertain.

Dielectrics	DIELECTRIC CONSTANT	E_g [eV]	Thermal conductivity [W/m•°K]
HfO_2 (or Hf)	20 ~ 25	6	23
Al_2O_3 (or Al)	7 ~ 9	8.8	35
SiO_2 (or Si)	3.9	9	1.5
BeO (or Be)	6.9	10.6	300

Table I. Summary of the material properties of HfO_2, Al_2O_3, SiO_2, and BeO dielectrics.

In table I, BeO has the highest thermal conductivity, which is related to the high S_{th}. Therefore, the total entropy of BeO may be greater than the other dielectrics. The higher the entropy, the higher thermal stability is. In general, higher thermal stability is preferred, even though the correlation between thermal stability and interface quality is still uncertain.

An Ellingham diagram is a graph showing the temperature dependence of the stability for compounds. This analysis is usually used to evaluate the ease of reduction of metal oxides and sulphides. In metallurgy, the Ellingham diagram is used to predict the equilibrium temperature between a metal, its oxide and oxygen, and by extension, reactions of a metal with sulphur, nitrogen, and other non-metals. The analysis is thermodynamic in nature and ignores reaction kinetics. Thus, processes that are predicted to be favorable by the Ellingham diagram can still be slow. Ellingham diagrams follow from the second law of thermodynamics [$\Delta G = \Delta H - T\Delta S$] and are a particular graphical form of it. ΔG is the Gibbs Free Energy Change, ΔH is the Enthalpy Change and ΔS is the Entropy Change.

The Ellingham diagram plots the Gibbs free energy change (ΔG) for the oxidation reaction versus the temperature. In the temperature ranges commonly used, the metal and the oxide are in a condensed state (liquid or solid) with the oxygen gaseous, the reactions may be exothermic or endothermic, but the ΔG of the oxidation always becomes more negative with lower temperature, and thus the reaction becomes more probable statistically. At a sufficiently high temperature, the sign of ΔG may invert (becoming negative) and the oxide can spontaneously reduce to the metal. Fig 1 is the Ellingham diagram of three dielectric formations, and Table II is the reaction equation which is calculated from Ellingham diagram, respectively. From these calculations, BeO reaction shows more negative ΔG, and it is the indication of high thermal stability, compared to other two dielectrics.

In summary, we suggested a theoretical model that, using electromagnetic theory and Langevin theory, highlights the electromagnetic interactions between the channel carrier and atoms in the gate dielectric, as well as the structural stability of the gate dielectric. From this model and the thermal stability of materials, we have found that BeO may be useful as an interfacial layer for Si, Ge, SiGe and III-V MOS devices. This is the background of the BeO birth.

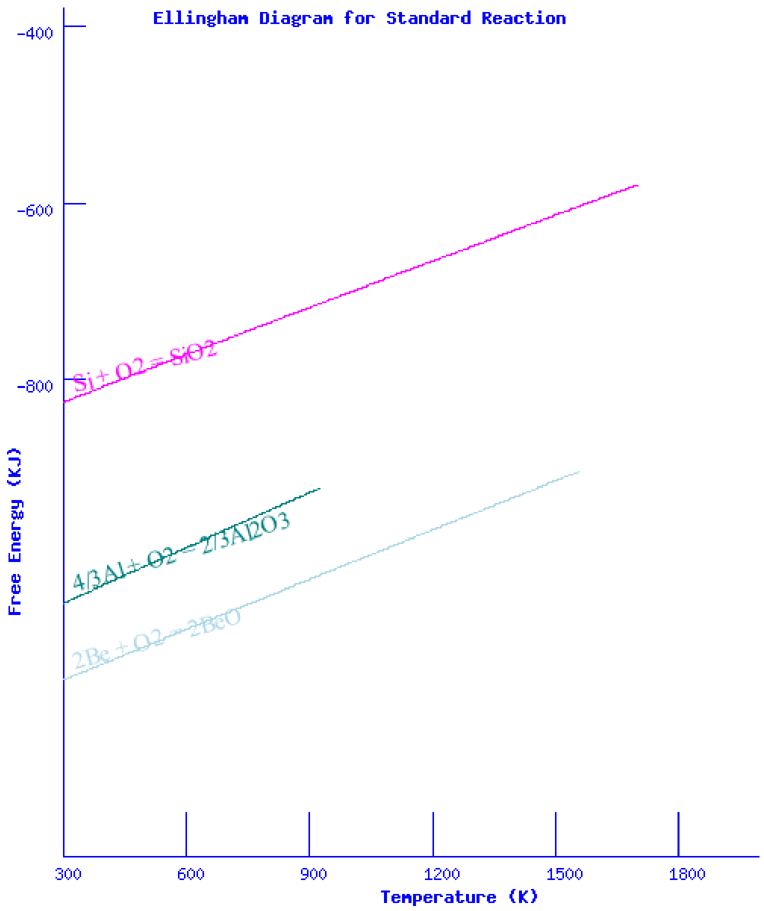


Fig 1. Ellingham diagram of Al_2O_3, BeO, and SiO_2 dielectrics for standard reaction.

❑ $2Al(CH_3)_3 + 3H_2O \rightarrow Al_2O_3 + 3CH_4$ $\Delta H = -376kcal$

❑ $3Be(CH_3)_2 + 3H_2O \rightarrow 3BeO + 6CH_4$ $\Delta H = -409kcal$

Table III. The reaction equations for Al_2O_3 and BeO ALD growth.

Reference

Chapter 1

[1] C.T. Liu, "Circuit Requirement and Integration Challenges of Thin Gate Dielectrics for Ultra Small MOSFETs," *IEDM Tech. Dig*., p. 174, (1998)

[2] P. J. Wright, and K. C. Saraswat, "Thickness Limitations for SiO2 Gate Dielectrics for MOS ULSI," *IEEE Trans. Electron Devices*, Vol. 37, p. 1884, Aug (1990)

[3] I. Ok, H. Kim, M. Zhang, F. Zhu, S. Park, J. Yum, H. Zhao and Jack C. Lee, "Temperature effects of Si interface passivation layer deposition on high-k III-V metal-oxide-semiconductor characteristics," *Applied Physics Letters* **91**, 132104 (2007)

[4] J. J. H. Gielis, B. Hoex, M. C. M. van de Sanden, and W. M. M. Kessels, "Effective passivation of Si surfaces by plasma deposited SiOx/a-SiNx:H stacks," *Applied Physics Letters* **104**, 073701 (2008)

[5] D. Shahrjerdi, M. M. Oye, Archie L. Holmes, Jr and S. K. Banerjee, "Unpinned metal gate/high-κ GaAs capacitors: Fabrication and characterization," *Applied Physics Letters* **89**, 043501 (2006)

[6] Davood Shahrjerdi, Emanuel Tutuc and Sanjay K. Banerjee, "Impact of surface chemical treatment on capacitance-voltage characteristics of GaAs metal-oxide-semiconductor capacitors with Al_2O_3 gate dielectric," *Applied Physics Letters* **91**, 063501 (2007)

[7] D. I. G. Gutierrez, D. Shahrjerdi, V. Kaushik and S. K. Banerjee, "Physical and electrical characterizations of metal-oxide-semiconductor capacitors fabricated on GaAs substrates with different surface chemical treatments and Al_2O_3 gate dielectric," *J. Vac. Sci. Technol*. B **27**, 2390 (2009)

[8] K. J. Hubbard and D. G. Schlom, "Thermodynamic stability of binary oxides in contact with silicon," *J. Mater. Res*, **11**, 11 (1996)

[9] C. W. Cheng, J. Hennessy, D. Antoniadis and E. A. Fitzgerald, "Self-cleaning and surface recovery with arsine pretreatment in *ex situ* atomic-layer-deposition of Al_2O_3 on GaAs," *Applied Physics Letters* **95**, 082106 (2009)

[10] Ira N. Levine, "Quantum chemistry 4rd edition" text book p 387–517, 646–700

[11] G. Lucovsky, H. Seo, S. Lee, L. B. Fleming, M. D. Ulrich, J. Lüning, P. Lysaght, and G. Bersuker, Japan. "Intrinsic Electronically Active Defects in Transition Metal Elemental Oxides," *J. Applied Physics*, **46**, 1899-1909 (2007)

[12] V. A. Sashin, M. A. Bolorizadeh, A. S. Kheifets and M. J. Ford, "Electronic band structure of beryllium oxide," *J. Phys.: Condens. Matter* **15** 3567 (2003)

[13] American Beryllia inc, This resource provides the electrical and mechanical properties of BeO. See: http://www.americanberyllia.com/

[14] G. E. Coates, F. Glockling and N. D. Huck, "Dimethylberyllium. Part I. Vapour pressure and vapour-phase association," *J. Chem. Soc.*, **1952**, 4496-4501

[15] H. Gilman, F. Schulze, F. *J. Chem. Soc.*2663-2669 (1927)

Chapter 2

[1] S. Devanarayanan, G. Morel1 and R. S. Katiyart, "Raman spectroscopy of BeO at low temperatures," *J. Raman Spectroscopy*, **22**, 311-314 (1991)

[2] A. Bosak, K. Schmalzl, M. Krisch, W. V. Beek, and V. Kolobanov, "Lattice dynamics of beryllium oxide: Inelastic x-ray scattering and *ab initio* calculations," *Physical Review B*, **77**, 224303 (2008)

[3] G. Morell, "*Anharmonic Interactions in Beryllium Oxide*," *Physical Review B*, **53**, 9 (1996)

[4] XPS database for Be 1s, See: http://www.lasurface.com/database/elementxps.php

[5] K. J. Hubbard and D. G. Schlom, "Thermodynamic stability of binary oxides in contact with silicon," *J. Mater. Res*, **11**, 11 (1996)

[6] American Beryllia inc, This resource provides the electrical and mechanical properties of BeO. See: http://www.americanberyllia.com/

[7] D.R.G. Mitchell, D. J. Attard, and G. Triani, "Transmission electron microscopy studies of atomic layer deposition TiO_2 films grown on silicon," *Thin solid films*, **441,** 85-93 (2003)

[8] J. E. Jaffe, P. Zapol, "Atomic relaxation of the BeO (1010) surface," *Surface Science*, **381,** 563 ~ 567 (1997)

[9] J. H. Yum, T. Akyol, M. Lei, T. Hudnall, G. Bersuker, M. Downer, C. W. Bielawski, J. C. Lee and S. K. Banerjee, "Atomic layer deposited beryllium oxide: Effective passivation layer for III-V metal/oxide/semiconductor devices," *J. Appl. Phys*. **109**, 064101 (2011).

Chapter 3

[1] D. Liu, J. Robertson, "Passivation of oxygen vacancy states and suppression of Fermi pinning in HfO_2 by La addition," *Applied Physics Letters.* **94**, 042904 (2009).

[2] D. Liu, S. J. Clark, and J. Robertson, "Oxygen vacancy levels and electron transport in Al_2O_3," *Applied Physics Letters.* **96**, 032905 (2010).

[3] A. Marnetto, M. Penna, F. Bertazzi, E. Bellotti, M. Goano, "*Ab initio*, nonlocal pseudopotential, and full-zone $k{\cdot}p$ computation of the electronic structure of wurtzite BeO," *Opt Quant Electron*, **40**, 1135–1141 (2008)

[4] N. N. Eremin, N. A. Gromalova, and V. S. Urusov, "Atomic modeling and prediction of the structure, energy characteristics of point defects, and thermodynamic and elastic properties of the simple and complex beryllium oxides," *Glass Physics and Chemistry*, **35**, 613–619 (2009).

[5] S. Lim, S. Kriventsov, T. N. Jackson, J. H. Haeni, D. G. Schlom, A. M. Balbashov, R. Uecker, P. Reiche, J. L. Freeouf, and G. Lucovsky, "Dielectric functions and optical bandgaps of high-K dielectrics for metal-oxide-semiconductor field-effect transistors by far ultraviolet spectroscopic ellipsometry,"*J. Appl. Phys*. 91, 4506 (2002).

[6] V. V. Afanaseva and A. Stesmans, "Internal photoemission at interfaces of high-κ insulators with semiconductors and metals," *J. Applied Physics*. **102**, 081301 (2007)

[7] H. Jin, S. K. Oh, H. J. Kang, Y. S. Lee and M. H. Cho, "Temperature dependence of band alignments in ultrathin Hf–Al–O and Al_2O_3 films on *p*-Si (100)," *Surf. Interface Anal*, **38**, 502–505 (2006)

[8] T. Minegishi, T. Hanada, H. Suzuki, Z. Vashaei, D. C. Oh, K. Sumitani, O. Sakata, M. W. Cho, T. Yao, "Structural characterization of MgO/c-Al_2O_3 interfaces," *Physica Status Solidi (c)*, **5**, 1715–1718 (2007)

[9] B. Qi, B. Agnarsson, K. Jonsson, S. Olafsson and H.P. Gislason, "Characterisation of high-temperature annealing effects on α—Al_2O_3(0001) substrates," *Journal of Physics: Conference Series*, **100,** 042020 (2008)

[10] A. Argoitia, J. C. Angus, L. Wang, X. I. Ning, P. Pirouz, "Diamond grown on single-crystal beryllium oxide," *J. Applied Physics* **73**, 4305 (1993).

[11] D. Yang, M. Krasowska, R. Sedev, and J. Ralston, "The unusual surface chemistry of α-Al_2O_3 (0001)," *Phys. Chem. Chem. Phys.*, **12**, 13724-13729, (2010)

[12] S.P. Taguchi, F.V. Motta, R. M. Balestra, S. Ribeiro, "Wetting behaviour of SiC ceramics Part II—Y_2O_3/Al_2O_3 and Sm_2O_3/Al_2O_3," *Materials Letters*, **58**, 2810– 2814, (2004)

[13] M. Ohring, "Material Science of Thin Films", 2nd edition (chapter 7)

[14] R. Katamreddy, R. Inman, G. Jursich, A. Soulet, and C. Takoudis, "Controlling interfacial reactions between HfO2 and Si using ultrathin Al2O3 diffusion barrier layer," *Appl. Phys. Lett* **89**, 262906 (2006).

[15] American Beryllia inc, This resource provides the electrical and mechanical properties of BeO. See: http://www.americanberyllia.com/

[16] J. H. Yum, T. Akyol, M. Lei, T. Hudnall, G. Bersuker, M. Downer, C. W. Bielawski, J. C. Lee and S. K. Banerjee, "Atomic layer deposited beryllium oxide: Effective passivation layer for III-V metal/oxide/semiconductor devices," *J. Applied Physics* **109**, 064101 (2011).

[17] Ira N. Levine, "Quantum chemistry 4th edition" text book p 387–517, 646–700

[18] C. L. Hinkle, A. M. Sonnet, E. M. Vogel, S. McDonnell, G. J. Hughes, M. Milojevic, B. Lee, F. S. Aguirre-Tostado, K. J. Choi, H. C. Kim, J. Kim, and R. M. Wallace, "GaAs interfacial self-cleaning by atomic layer deposition," *Applied Physics Letter* **92**, 071901 (2008)

[19] C. L. Hinkle, M. Milojevic, E. M. Vogel and R. M. Wallace, ", The significance of core-level electron binding energies on the proper analysis of InGaAs interfacial bonding," *Applied Physics Letter,* **95**, 151905 (2009)

[20] K. Morimoto, T. Takagi, and H. Watanabe, "Method for producing a beryllium oxide film," U.S. Patent 4 451 499, May 29, 1984.

[21] I. Tanaka, I. Kamiya, H. Sakaki, N. Qureshi, S. J. Allen, Jr., and P. M. Petroff, “Imaging and probing electronic properties of self-assembled InAs quantum dots by atomic force microscopy with conductive tip,” *Appl. Phys. Lett.*, 74, 844 (1999)

[22] I. Tanaka, E. Kawasaki, O. Ohtsuki, K. Uno, M. Hara, H. Asami, and I. Kamiya, “Improved height measurement of single CdSe colloidal quantum dots by contact-mode atomic force microscopy using carbon nanotube tips; for the investigation of current-voltage characteristics,” *Jpn. J. Appl. Phys.*, vol. 44, no. 7, pp. L249–L252, Jan. 2005.

[23] V. Da Costa, C. Tiusan, T. Dimopoulos, and K. Ounadjela, “Tunneling phenomena as a probe to investigate atomic scale fluctuations in metal/oxide/metal magnetic tunnel junctions,” *Phys. Rev. Lett.*, vol. 85, no. 4, pp. 876–879, Jul. 2000.

[24] M. A. Alam, D. Varghese, and B. Kaczer, “Theory of breakdown position determination by voltage- and current-ratio methods,” *IEEE Trans. Electron Devices*, vol. 55, no. 11, pp. 3150–3158, Nov. 2008.

[25] J. S. Lewis and M. S. Weaver, “Thin-film permeation-barrier technology for flexible organic light-emitting devices,” *IEEE J. Sel. Top. Quantum Electron*. **10**, 45 (2004).

[26] T. Hirvikorpi, M. Vähä-Nissi, J. Nikkola, A. Harlin, and M. Karppinen, ” Thin Al2O3 barrier coatings onto temperature-sensitive packaging materials by atomic layer deposition,” *Surface & Coatings Technology* 205 (2011) 5088–5092

[27] H. Chatham, “Oxygen diffusion barrier properties of transparent oxide coatings on polymeric substrates,” *Surface & Coatings Technology* 78 (1996) 1–9

[28] M. S. Weaver, L. A. Michalski, K. Rajan, M. A. Rothman, J. A. Silvernail, J. J. Brown, P. E. Burrows, G. L. Graff, M. E. Gross, P. M. Martin, M. Hall, E. Mast, C. Bonham, W. Bennett, and M. Zumhoff, “Organic light-emitting devices with extended operating lifetimes on plastic substrates,” *Appl. Phys. Lett*. **81**, 2929 (2002).

[29] K. Lahtinen, P. Maydannik, P. Johansson, T. Kääriäinen, D. C. Cameron, and J. Kuusipalo, “Utilisation of continuous atomic layer deposition process for barrier enhancement of extrusion-coated paper,” *Surface & Coatings Technology* 205 (2011) 3916–3922

[30] G. L. Graff, R. E. Williford, and P. E. Burrows, “Mechanisms of vapor permeation through multilayer barrier films: Lag time versus equilibrium permeation,” *J. Appl. Phys*. **96**, 1840 (2004).

[31] M. Ritala and M. Leskela, in *Handbook of Thin Film Materials*, edited by H. S. Nawla (Academic, San Diego, 2001), **1**, p. 103.

[32] M. Ritala, J. Niinisto, in: A.C. Jones, M.L. Hitchman (Eds.), Chemical Vapour Deposition: Precursors, Processes and Applications, Royal Society of Chemistry, 2009, p. 158 (Chapter 4).

[33] M. Ritala, M. Leskela, in: H.S. Nalwa (Ed.), Handbook of Thin Film Materials, vol.1, Academic Press, San Diego, 2001, p. 103 (Chapter 2).

[34] R. Matero, M. Ritala, M. Leskela, T. Salo, J. Aromaa, O. Forsen, J. Phys. IV, 9 (Pr8) 493–499 (1999).

[35] C.X. Shan, X. Hou, K.L. Choy, “Corrosion resistance of TiO2 films grown on stainless steel by atomic layer deposition,” *Surf. Coat. Technol*. **202** 2399–2402 (2008).

[36] B. Diaz, J. S. wiatowska, V. Maurice, A. Seyeux, B. Normand, E. Harkonen, M. Ritala, P. Marcus, Electrochim. Acta. doi:10.1016/j.electacta.2011.02.074.

[37] X. Du, K. Zhang, K. Holland, T. Tombler, M. Moskovits, “Chemical corrosion protection of optical components using atomic layer deposition,” *Appl. Opt*. 48 6470–6474 (2009).

[38] W.M.M. Kessels, S.B.S. Heil, E. Langereis, J.L. van Hemmen, H.C.M. Knoops, W. Keuning, M.C.M. van de Sanden, “Opportunities for plasma-assisted atomic layer deposition,” *ECS Trans*. **3** 183–190 (2007).

[39] S.E. Potts, W. Keuning, E. Langereis, G. Dingemans, M.C.M. van de Sanden, W.M.M. Kessels, “Low Temperature Plasma-Enhanced Atomic Layer Deposition of Metal Oxide Thin Films,” *J. Electrochem. Soc*. **157** 66–74 (2010).

[40] H. B. Profijt, S. E. Potts, M. C. M. van de Sanden, and W. M. M. Kessels, “Plasma-Assisted Atomic Layer Deposition: Basics, Opportunities, and Challenges,” *J. Vac. Sci. Technol. A* **29**, 050801 (2011);

[41] J. H. Yum, T. Akyol, M. Lei, D. A. Ferrer, T. W. Hudnall, M. Downer, C. W. Bielawski, G. Bersuker, J. C. Lee and S. K. Banerjee, “Inversion type InP metal oxide semiconductor field effect transistor using novel atomic layer deposited BeO gate dielectric,” *Appl. Phys. Lett.* **99**, 033502 (2011)

[42] A. A. Dameron, S. D. Davidson, B. B. Burton, P. F. Carcia, R. S. McLean, and Steven M. George, “Gas Diffusion Barriers on Polymers Using Multilayers Fabricated by Al_2O_3 and Rapid SiO_2 Atomic Layer Deposition,” *J. Phys. Chem. C*, ***112***, 4573-4580 (2008).

[43] SRIM software for the collision simulation. http://www.srim.org/

Chapter 4

[1] J. Huang, P. D. Kirsch, J. W. Oh, S. H. Lee, P. Majhi, H. R. Harris, D. C. Gilmer, G. Bersuker, H. Dawei, C. S. Park, C. Park, H. H. Tseng, R. Jammy, “Mechanisms Limiting EOT Scaling and Gate Leakage Currents of High- k/Metal Gate Stacks Directly on SiGe,” *Electron Device Letters, IEEE,* **30**, 285-287 (2009)

[2] C. Marchiori, M. M. Frank, J. Bruley, V. Narayanan, and J. Fompeyrine, "Epitaxial SrO interfacial layers for HfO_2–Si gate stack scaling," *Appl. Phys. Lett.* **98**, 052908 (2011)

[3] T. Ando, M. Copel, J. Bruley, M. M. Frank, H. Watanabe, and V. Narayanan, " Physical origins of mobility degradation in extremely scaled SiO_2/HfO_2 gate stacks with La and Al induced dipoles," *Applied Physics Letters*, **96**, 132904 (2010).

[4] J. J. H. Gielis, B. Hoex, V. D. Sanden, M. C. M. van de Sanden, W. M. M. Kessels, " Negative charge and charging dynamics in Al_2O_3 films on Si characterized by second-harmonic generation," *J. Appl. Phys*. **104**, 073701 (2008).

[5] Cheng-Wei Chenga and Eugene A. Fitzgerald, "Improved interfacial state density in Al_2O_3/GaAs interfaces using metal-organic chemical vapor deposition,"*Applied Physics Letters*, **96**, 202101 (2010).

[6] C. L. Lin, M. Y. Chou, T. K. Kang, and S. C. Wu, " Electrical characteristics and TDDB breakdown mechanism of N_2-RTA-treated Hf-based high-κ gate dielectrics," *Microelectronic Engineering*, **88**, 950–958 (2011)

[7] M. Jo, H. K. Park, M. Chang, H. S. Jung, J. H. Lee, and H. S. Hwang, "Oxygen vacancy induced charge trapping and positive bias temperature instability in HfO2 nMOSFET," *Microelectronic Engineering*, **84**, 1934–1937 (2007)

[8] S. Jakschik, U. Schroedera, T. Hechta, M. Gutschea, H. Seidla, J. W. Barthab, "Crystallization behavior of thin ALD-Al_2O_3 films," *Thin Solid Films,* **425** 216–220 (2003)

Chapter 5

[1] K. J. Hubbard and D. G. Schlom, “Thermodynamic stability of binary oxides in contact with silicon,” J. Mater. Res. **11**, 2757 (1996).

[2] G. S. Lujan, S. Kubicek, S. De Gendt, M. Heyns, W. Magnus, and KA. De Meyer, “Mobility degradation in high-k transistors: the role of the charge scattering,” *ESSDERC* Conf (2003) pp 399 - 402

[3] Y. Kim *et a*l., “Conventional n-Channel MOSFET Devices Using Single Layer HfO2 and ZrO2 as High-k Gate Dielectrics with Polysilicon Gate Electrode”, *IEDM Techn. Dig.*, pp. 455-458, 2001.

[4] A. E. Islam, V. D. Maheta, H. Das, S. Mahapatra, and M. A. Alam, “Mobility degradation due to interface traps in plasma oxynitride PMOS devices,” *IRPS* 2008. pp 87 - 96

[5] M. Fischetti, D. Neumayer and E. Cartier, “Effective electron mobility in Si inversion layers in metal–oxide–semiconductor systems with a high-κ insulator: The role of remote phonon scattering,” *J. Appl. Phys*. **90**, 4587 (2001)

[6] J. H. Yum, T. Akyol, M. Lei, T. Hudnall, G. Bersuker, M. Downer, C. W. Bielawski, J. C. Lee and S. K. Banerjee, ”Atomic layer deposited beryllium oxide: Effective passivation layer for III-V metal/oxide/semiconductor devices,” J. Appl. Phys., 109, 064101 (2011)

[7] J. H. Yum, T. Akyol, M. Lei, D. A. Ferrer, T. Hudnall, G. Bersuker, M. Downer, C. W. Bielawski, J. C. Lee and S. K. Banerjee, “A study of highly crystalline novel beryllium oxide film using atomic layer deposition,” J. Crystal. Growth. 334 (2011) 126-133

[8] J. H. Yum, T. Akyol, M. Lei, D. A. Ferrer, T. Hudnall, G. Bersuker, M. Downer, C. W. Bielawski, J. C. Lee and S. K. Banerjee, "Inversion type InP metal oxide semiconductor field effect transistor using novel atomic layer deposited BeO gate dielectric," Appl. Phys. Lett., 99, 033502 (2011)

[9] J. H. Yum, T. Akyol, M. Lei, D. A. Ferrer, T. Hudnall, G. Bersuker, M. Downer, C. W. Bielawski, J. C. Lee and S. K. Banerjee, "Comparison of the self-cleaning effects and electrical characteristics of BeO and Al2O3 deposited as an interface passivation layer on GaAs MOS devices," J. Vac. Sci. Technol. A 29, 061501 (2011)

[10] J. H. Yum, T. Akyol, M. Lei, K.W. Park, Todd. W. Hudnall, M. Downer, C. W. Bielawski, G. Bersuker, E. T. Yu, J. Price, J. C. Lee and S. K. Banerjee, "Epitaxial ALD BeO: Efficient Oxygen Diffusion Barrier for EOT Scaling and Reliability Improvement." IEEE *Electron Device Lett*, In Press 2011

[11] Rolf E. Hummel, "Electronic Properties of Materials", 3rd edition, chap 21, page 394−395.

[12] A. A. Dameron, S. D. Davidson, B. B. Burton, P. F. Carcia, R. S. McLean, and Steven M. George, "Gas Diffusion Barriers on Polymers Using Multilayers Fabricated by Al_2O_3 and Rapid SiO_2 Atomic Layer Deposition," *J. Phys. Chem. C*, ***112***, 4573-4580 (2008).

[13] David R. Gaskell, "Introduction to the Thermodynamics of materials", 5th edition, chap 4, page 69−83

[14] Ben G. Streetman, Sanjay Kumar Banerjee, "Solid State Electronic Devices" 6th edition, page 272−273.

[15] S. J. Rhee, C. Y. Kang, C. S. Kang, R. Choi, C. H. Choi, M. S. Akbar, and J. C. Lee, "Effects of varying interfacial oxide and high-*k* layer thicknesses for HfO_2 metal–oxide–semiconductor field effect transistor," *Appl. Phys. Lett*. 85, 1286 (2004).

Chapter 6

[1] L. G. Meiners, in Physics and Chemistry of III-V Compound Semiconductor interfaces, edited by C. W. Wilmsen (Plenum. New York, 1985), p 213.

[2] L. MEINERS, D. L. LILE, and D. A. COLLINS, “Microwave gain from an /i-channel enhancement-mode InP MISFET,” Elec. Dev. Lett., 1979, 15, p. 578

[3] T. KAWAKAMI, and M. OKAMURA, “JV-channel formation on semi insulating InP surface by MISFET,” ibid., 1979,15, p 743

[4] D. FRITZSCHE, D. “Interface studies on InP MIS inversion FETs with SiO_2 gate Insulation,”. Inst. Phys. conf. serial no. 50, 1980, pp. 258-265

[5] J. WOODWARD, D. C. CAMERON, I. D. IRVING, and G. R. JONES, “The deposition of insulators on InP using PECVD\ Thin Solid Films,” 1981,85, pp. 61-69

[6] L. HENRY, D. LECROSNIER, H. L'HARIDON, J. PAUGAM, G. PELOUS, F. RICHOU, and M. SALVI, “W-channel MISFETs on semi-insulating InP for logic applications”, Elec. Dev. Lett., 1982, 18, p. 102

[7] L. G. Meiners, J. Yac Sci. Technol. 21, 655 (1982).

[8] K. P. Pande, V. R. K. Nair, and O. Aina, “Capless annealing of InP for metal-insulator-semiconductor field-effect transistor applications”, Appl. Phys. Lett. 45, 532 (1984)

[9] R. Lyer and D. Lite, I. Electrochem. 135, 691 (1988).

[10] A. A. Lakhani, Solid-State Electron. 27, 921 (1984).

[11] B. R. Bennett, K, Veccaro, 3. P. Loremzo, K. M. Sleboda, and A. Davis, J. Electron. Mater. 17, 365 (1988).

[12] H. M. Kim, S. S. Tai, S. L. Groves, and K. K. Schuegraf, Proceedings of the 8th International Conference on CVD (Electrochemical Society, New Jersey, 1981), p. 258.

[13] M. Okuyama, Y. Toycda, and Y. Hamakawa, Jpn. J. Appl. Phys. 23,97 (1984).

[14] Y. Shacham-Diamand, N. Moriya, G. Bahir, "Electronic properties of metal/solgel SiOzlinciium-phosphode capacitor", Appl. Phys. Lett. 58 (12), 25 March 1991

[15] G. W. Anderson, M. C. Hanf, P. R. Norton, Z. H. Lu and M. J Graham, " Thermal stability of surfur passivated in (100)-(1X1)", Applied Physics Letters, 65, 11 July (1994)

[16] D. Landheer, G. H. Yousefi, and J. B. Webb, R. W. M. Kwok and W. M. Lau, "Deep-level transient spectroscopy of Hf-cleaned and surfur-passivated InP metal/nitride/semiconductor structures", Journal of Applied Physics, 75 (7), 1 April 1994

[17] M. Shimomura, K. Naka, N. Sanada, Y. Suzuki, and Y. Fukuda,and P. J. Moller, "Surface structures and electronic states of H2S-treated InP (001)", Journal of Applied Physics, 79 (8), 15 April 1995

[18] Yun Sun, Zhi Liu, Francisco Machuca, Piero Pianetta, and William E. Spicer, "Optimized cleaning method for producing device quality InP (100) surface", Journal of Applied Physics, 97 124902 (2005)

[19] Yu-Shyan Lin and Jr-Hung Huang, "Mobility Enhancement and Breakdown Behavior in InP-Based Heterostructure Field-effect Transistor", Journal of The Electrochemical Society, 152 (8) G627-G629 (2005)

[20] D. Lubyshev, J. M. Fastenau, X.-M. Fang, Y. Wu, C. Doss, A Snyder, W. K. Liu, M. S. M. Lamb, S. Bals and C. Song, "Comparison of As-and P-based metamorphic buffers for high performance InP heterojunction bipolar transistor and high electron mobility transistor applications." J. Vac. Sci. Technol. B 22(3), May/Jun 2004

[21] S. Ingrey, "III-V surface processing", J. Vac. Sci. Technol. A 10(4), Jul/Aug 1992

[22] I. A. Buyanova, W. M. Chen, W. G. Bi, Y. P. Zeng, and C. W. Tu, "Thermal stability and doping efficiency of intrinsic modulation doping in InP-based structures", Applied Physics Letters, 75(12), 20 September (1999)

[23] Zhi Jin, W. Prost, S. Neumann, and F. J. Tegude, "Current transport mechanisms and their effects on the performances of InP-based double heterojunction bipolar transistors with different base structures." Applied Physics Letters 84(15) 2004

[24] T. P. Chin, Y. C. Chen, M Barsky, M. Wojtowicz, R. Grundbacher, R. Lau, D. C. Streit, and T. R. Block, " High performance InP high electron mobility transistors by valved phosphorus cracker" J. Vac. Sci. Technol. B 18(3), May/Jun 2000

[25] Y. Q. Wu, Y. Xuan, P. D. Ye, Z. Cheng, A. Lochtefeld, "Inversion-type enhancement-mode InP MOSFETs with ALD Al_2O_3, HfO_2 and HfAlO nanolaminates as high-k gate dielectrics", in IEEE Device Research Conference, 2007

[26] J. H. Yum, T. Akyol, M. Lei, T. Hudnall, G. Bersuker, M. Downer, C. W. Bielawski, J. C. Lee and S. K. Banerjee, “Atomic layer deposited beryllium oxide: Effective passivation layer for III-V metal/oxide/semiconductor devices,” *J. Appl. Phys*. 109, 4 (2011)

[27] Y. Q. Wu, Y. Xuan, T. Shen, and P. D. Yea, *Applied Physics letters* 91, 022108 (2007)

[28] H. Zhao, D. Shahrjerdi, F. Zhu, H. S. Kim, I. Ok, M. Zhang, J. H. Yum, S. K. Banerjee and J. C. Lee, *Electrochemical and Solid-State Letters,* 11 (8) H233-H235 (2008)

Chapter 7

[1] J. H. Yum, T. Akyol, M. Lei, T. Hudnall, G. Bersuker, M. Downer, C. W. Bielawski, J. C. Lee and S. K. Banerjee, “Atomic layer deposited beryllium oxide: Effective passivation layer for III-V metal/oxide/semiconductor devices,” *J. Appl. Phys*., 109, 064101 (2011)

[2] J. H. Yum, T. Akyol, M. Lei, D. A. Ferrer, T. Hudnall, G. Bersuker, M. Downer, C. W. Bielawski, J. C. Lee and S. K. Banerjee, "A study of highly crystalline novel beryllium oxide film using atomic layer deposition," *J. Crystal. Growth*. 334 (2011) 126-133

[3] J. H. Yum, T. Akyol, M. Lei, D. A. Ferrer, T. Hudnall, G. Bersuker, M. Downer, C. W. Bielawski, J. C. Lee and S. K. Banerjee, "Inversion Type InP Metal Oxide Semiconductor Field Effect Transistor Using Novel Atomic Layer Deposited BeO Gate Dielectric," *Appl. Phys. Lett*., 99, 033502 (2011)

[4] J. H. Yum, T. Akyol, M. Lei, D. A. Ferrer, T. Hudnall, G. Bersuker, M. Downer, C. W. Bielawski, J. C. Lee and S. K. Banerjee, "Comparison of Self Cleaning Effect and Electrical Characteristics between Atomic Layer Deposited BeO and Al_2O_3 as an Interface Passivation Layer on GaAs MOS Devices," *J. Vac. Sci. Technol. A* 29, 061501 (2011)

[5] J. H. Yum, T. Akyol, M. Lei, K.W. Park, Todd. W. Hudnall, M. Downer, C. W. Bielawski, G. Bersuker, E. T. Yu, J. Price, J. C. Lee and S. K. Banerjee, "Epitaxial ALD BeO: Efficient Oxygen Diffusion Barrier for EOT Scaling and reliability improvement," Tran of Electron Device Vol. 58, pp. 4384−4392, No. 12, DEC (2011)

[6] M. Kundu, N. Miyata, and M. Ichikawa, "Study of ultrathin Al_2O_3/Si(001) interfaces by using scanning reflection electron microscopy and x-ray photoelectron spectroscopy," *Appl. Phys. Lett*. **78**, 1517 (2001).

[7] B. Lux, C. Colombier, H. Altena, and K. Stjernberg, "Preparation of alumina coatings by chemical vapour deposition," *Thin Solid Films* **138**, 49 (1986).

[8] A. D. Becke, "A new mixing of Hartree–Fock and local density-functional theories," *J. Chem. Phys*. **98**, 1372 (1993).

[9] Ira. N. Levine, "*Quantum Chemistry*," pp. 461–466. (1991).

[10] Molecular Modeling Tools for Chemistry; Spartan 08, http://www.wavefun.com

[11] Y. Widjaja, and C. B. Musgravea, "Quantum chemical study of the mechanism of aluminum oxide atomic layer deposition," *Appl. Phys. Lett.*, **80**, 3304 (2002)

[12] G. A. Balueva, and S. T. Ioffe, "Organic compounds of Beryllium, Calcium, Strontium, and Barium," *Russ. Chem. Rev*. 31 439 (1962)

[13] Catherine E. Housecroft and Alan G. Sharpe, "Inorganic Chemistry" 3rd chapter 12

[14] F. A. Cotton, G. Wilkinson, and C. Murillo, Advanced Inorganic Chemistry, 6th ed. (Wiley, New York, 1999).

Appendix

[1] J. H. Yum, T. Akyol, M. Lei, D. A. Ferrer, T. Hudnall, G. Bersuker, M. Downer, C. W. Bielawski, J. C. Lee and S. K. Banerjee, "A study of highly crystalline novel beryllium oxide film using atomic layer deposition," J. Crystal. Growth, 334, p126-133 (2011)

[2] P. G. Klemens, "Thermal conductivity of inhomogeneous materials," *International Journal of Thermophysics, Vol. 10, No. 6* (1989)

Vita

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